Craignell2 User Manual

Issue – 1.0

Purchase Optional Extras

The following, or equivalent, are necessary to program a module.

1 – Prog2 or Prog3 Programming Cable.
2 – Craignell2 Programming Adapter

We also have ZIF based module to power a Craignell2 outside of a target board to allow programming. Contact boardsales@enterpoint.co.uk for more details on this item.

Foreword

PLEASE READ THIS ENTIRE MANUAL BEFORE PLUGGING IN OR POWERING UP YOUR CRAIGNELL2 BOARD.
PLEASE TAKE SPECIAL NOTE OF THE WARNINGS WITHIN THIS MANUAL.

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Contents

Introduction

Welcome to your Craignell2 board. Craignell2 is a low cost high performance Spartan™-3E FPGA based module.

The aim of this manual is to assist in using the main features of Craignell2. Should this manual fail to explain a feature sufficiently then our support team can be reached by email on support@enterpoint.co.uk.

Getting Started

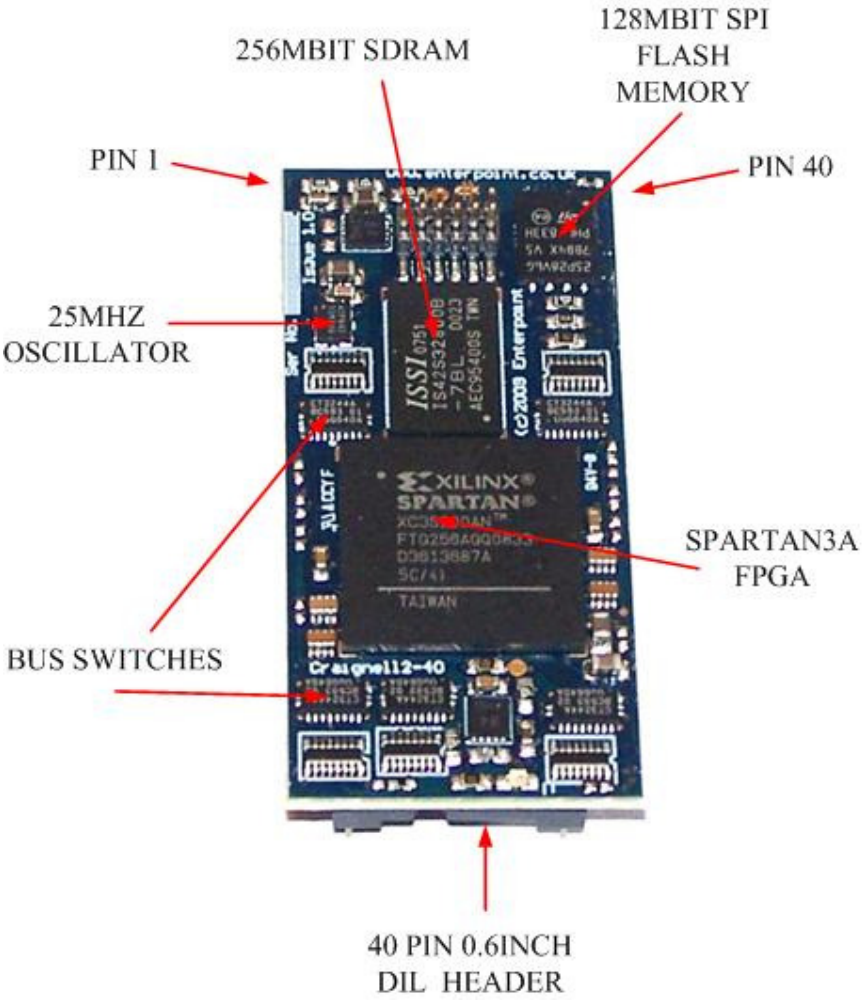
Craignell2 is currently available in 2 sizes – 40 pin and 48 pin. The FPGA fitted to Craignell2 is usually the XC3S700A-4FTG256C but Craignell2 modules based on 200A, 400A and 1400A versions of this device are available for special orders. Contact boardsales@enterpoint.co.uk for information.

Your Craignell2 normally comes with our LED Flash Test build loaded. This application will cause the LED to flash on and off and indicates power is applied, the on-board oscillator is running and the FPGA has configured from the on-board SPI Flash Memory.

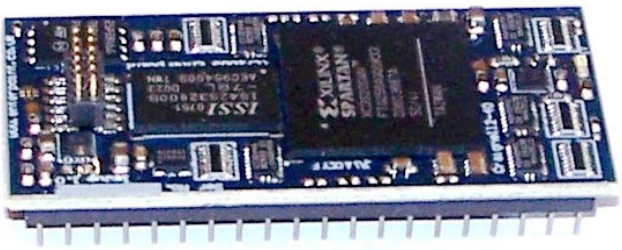
Pin1 of the module is on the back side of the module at the top left of the picture above (CR2-40). Pins count counter-clockwise from Pin1.

Craignell2 Features

Location of Components



Side View



Power Inputs and Power Supplies

Craignell2 normally uses a 5V input but can operate from 3.5V to 5.5V (specification guaranteed).

The pins on which the 5v and the 0V power connections are made to the Craignell2 can be selected by the addition of a small wire link or zero ohm resistor. The sites for these connections are very small (0402 size) so these connections should be made by a competent technician skilled in soldering at this technology. Enterpoint Ltd does not accept responsibility for damage to a Craignell2 module if such damage is caused by poor soldering.

Craignell2-40 is usually supplied with 5v connected on pin 40 and 0V connected on pin 20. Craignell2-48 is usually supplied to be used with 5v connected on pin 48 and 0V connected on pin 24. However the following alternative power supply configurations are available pre-configured for a small additional cost:

VOLTAGE	PINS AVAILABLE CR2-40	PINS AVAILABLE CR2-48
5V	7, 8, 9, 10, 11, 12, 15, 17, 20, 21, 23, 26, 31, 40.	7, 8, 9, 10, 11, 12, 13, 24, 29, 34, 39
0V	1, 7, 20, 21, 29, 30, 31	1, 7, 15, 17, 23, 24, 29, 36, 38, 39

Power Regulators

Two AP7167 regulators provide 3.3v and 1.2V to the FPGA. These regulators can provide a maximum of 1A each.

WARNING – THE REGULATORS CAN POTENTIALLY GET VERY HOT IN SOME UNUSUAL CIRCUMSTANCES ALONG WITH THE BOARDS THERMAL RELIEF. PLEASE DO NOT TOUCH OR PLACE HIGHLY FLAMABLE MATERIALS NEAR THIS DEVICE WHILST THE CRAIGNELL2 BOARD IS IN OPERATION.

Pin header I/O

The Craignell2 is fitted with a 0.1inch pitch 0.6inch wide DIL header with pins extending from the underside of the Craignell2 PCB to enable the Craignell module to become a plug-in replacement for an obsolete component or as a plug-in enhancement module for the user's own circuitry. Craignell2-40 has 40 pins and Craignell2-48 has 48 pins. The pins are connected to General purpose IO on the FPGA via bus switches so that 5V tolerance is achieved.

The Connections between the FPGA and the header pins are shown below. 2 of these connections will not be available to the user as IO because they will be required as power connections (5v and 0v) as described previously.

1. CR2-40

HEADER PIN	FPGA PIN	HEADER PIN	FPGA PIN
1	L1	21	T8
2	K1	22	T9
3	K3	23	R9
4	J1	24	P9
5	J2	25	P11
6	H1	26	T11
7	J3	27	R11
8	G1	28	T10
9	P2	29	R15
10	N2	30	R13
11	R3	31	T13
12	T4	32	P12
13	T5	33	C16
14	N8	34	D15
15	T7	35	D16
16	R7	36	E16
17	P8	37	F15
18	P7	38	F16
19	R5	39	H15
20	T6 (default 0v power)	40	G16 (default 5V power)

2. CR2-48

HEADER PIN	FPGA PIN	HEADER PIN	FPGA PIN
1	L1	25	M3
2	K1	26	K4
3	K3	27	M4
4	J1	28	L4
5	J2	29	T8
6	H1	30	T9
7	J3	31	R9
8	G1	32	P9
9	P2	33	P11
10	N2	34	T11
11	R3	35	R11
12	T4	36	T10
13	T5	37	R15
14	N8	38	R13
15	T7	39	T13

16	R7	40	P12
17	P8	41	C16
18	P7	42	D15
19	R5	43	D16
20	T6	44	E16
21	N13	45	F15
22	L13	46	F16
23	K13	47	H15
24	K14	48	G16 (default 5V power)

SDRAM

The Craignell2 has a 256Mbit SDRAM device type IS42S32800 fitted (or equivalent) which is configured as 2M Words x 32 Bits x 4 Banks. The device package it 90VBGA. For further information about this device please consult www.issi.com. The connections between the SDRAM and the FPGA are shown below:

SIGNAL NAME	SDRAM PIN	FPGA PIN		SIGNAL NAME	SDRAM PIN	FPGA PIN
SDRAM_DQ0	R8	E7		SDRAM_DQ29	D2	B8
SDRAM_DQ1	N7	D8		SDRAM_DQ30	D3	A8
SDRAM_DQ2	R9	C1		SDRAM_DQ31	E2	C8
SDRAM_DQ3	N8	D7		SDRAM_A0	G8	J12
SDRAM_DQ4	P9	D1		SDRAM_A1	G9	A3
SDRAM_DQ5	M8	G13		SDRAM_A2	F7	A7
SDRAM_DQ6	M7	G14		SDRAM_A3	F3	D10
SDRAM_DQ7	L8	C2		SDRAM_A4	G1	B12
SDRAM_DQ8	L2	F13		SDRAM_A5	G2	A12
SDRAM_DQ9	M3	D9		SDRAM_A6	G3	F14
SDRAM_DQ10	M2	E13		SDRAM_A7	H1	A13
SDRAM_DQ11	P1	D14		SDRAM_A8	H2	B14
SDRAM_DQ12	N2	D12		SDRAM_A9	J3	C7
SDRAM_DQ13	R1	B15		SDRAM_A10	G7	J13
SDRAM_DQ14	N3	C9		SDRAM_A11	H9	C4
SDRAM_DQ15	R2	C13		SDRAM_A12	H3	D11
SDRAM_DQ16	E8	B3		SDRAM_BA0	J7	F1
SDRAM_DQ17	D7	B6		SDRAM_BA1	H8	D4
SDRAM_DQ18	D8	A6		SDRAM_DQM0	K9	E2
SDRAM_DQ19	B9	B4		SDRAM_DQM1	K1	C15
SDRAM_DQ20	C8	A5		SDRAM_DQM2	F8	F3
SDRAM_DQ21	A9	A4		SDRAM_DQM3	F2	C12
SDRAM_DQ22	C7	C6		SDRAM_CLK	J1	A14
SDRAM_DQ23	A8	C5		SDRAM_CKE	J2	C11
SDRAM_DQ24	A2	B10		SDRAM_CS_N	J8	E3
SDRAM_DQ25	C3	A9		SDRAM_RAS_N	J9	D3
SDRAM_DQ26	A1	A11		SDRAM_CAS_N	K7	H13
SDRAM_DQ27	C2	C10		SDRAM_WE_N	K8	E1
SDRAM_DQ28	B1	A10				

FPGA

Craignell2 supports Spartan™-3A devices in the FTG256C package. Standard builds of Craignell2 use commercial grade devices but industrial grade parts can be fitted at extra cost subject to minimum order quantities and charges. The FPGA fitted to Craignell2 is usually the XC3S700A-4FTG256C but Craignell2 modules based on 200A, 400A and 1400A versions of this device are available for special orders. Contact boardsales@enterpoint.co.uk for information.

LED

Supplied on Craignell2 there is 1 LED driven by the FPGA. LED1 has a positive polarity i.e. '1' = on. The LED is connected to the FPGA on pin **N12**.

OSCILLATOR

Craignell2 comes fitted with a 25 MHz oscillator. This is connected to the FPGA on pin **N9.**

SPI FLASH MEMORY

Supplied as standard on Craignell2 is a 128Mbit SPI Flash memory device M25P128. This device is used to configure the Spartan™-3A. The remainder of flash memory is available for storing code for PicoBlaze™, MicroBlaze™ or other applications.

An XC3S700A will use 2,732,640 bits of this memory for configuration.

Programming Craignell2

For programming and building your design you will need a copy of Xilinx™ ISE software. Designs for Craignell2 can be implemented using the free Webpack™ version of ISE which can be downloaded from www.xilinx.com.

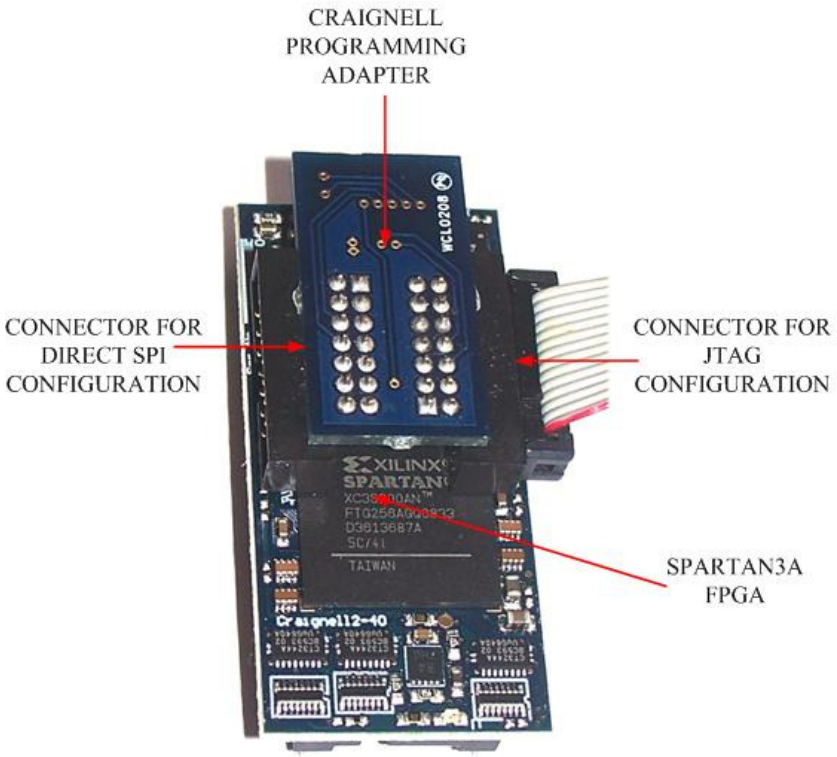
Programming of the FPGA and SPI Flash parts on Craignell2 is achieved using the JTAG interface. Principally it is anticipated that a JTAG connection will be used in conjunction with Xilinx ISE software although other alternatives do exist including self re-programming. The Spartan 3A series needs to be programmed using ISE 9 or higher. There are 2 ways of programming the Craignell2.

There is a single JTAG chain on Craignell2. The JTAG chain allows the programming of the Spartan-6 and SPI Flash device.

The JTAG connector is a 6x2 1.27mm header which has a layout as follows (top view):

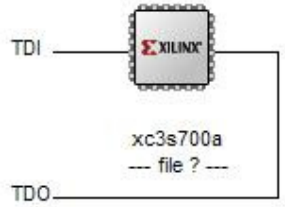
3V3	**PROG_B**	**CCLK**	**DIN**	**MOSI**	**CSO_B**
3V3	**GND**	**TCK**	**TDO**	**TDI**	**TMS**

The JTAG signals are shown in red, the Direct SPI configuration signals are green. In order to program the Craignell2 it is necessary to use a Craignell Programming adapter which separates out these 2 sets of signals and routes them to 2 standard 2x7x2mm IDC connectors which can be used by all standard Xilinx and Enterpoint programming cables. The adapter should be fitted to the Craignell2 as shown below:



Power-up the Craignell2 module. Plug in your programming cable to the JTAG configuration connector on the Craignell programming adapter. Plug the Craignell programming adapter into the Craignell2, taking care that the 6x2 connectors are correctly aligned.

Using iMPACT Boundary Scan the JTAG chain appears like this:



1. Programming the FPGA directly.

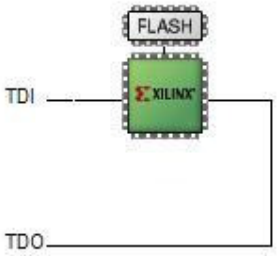
Direct JTAG programming of the Spartan-3A FPGA is volatile and the FPGA will lose its configuration every time the board power is cycled. For sustained use of an FPGA design programming the design into the Flash memory is recommended (see 2 and 3 below).
Direct JTAG programming using .bit files is useful for fast, temporary programming during development of FPGA programs.

Right click the icon representing the Spartan-3A FPGA and choose 'Assign New Configuration File'. Navigate to your .bit file and choose 'OPEN'. The next dialogue box may offer to add a flash memory and you should decline. Right click the icon representing the Spartan-3A FPGA and choose 'Program'. On the next dialogue box ensure that the 'Verify' box is not checked. (If it is you should uncheck it, failure to do this will result in error messages being displayed). Click OK. The Spartan-3A will program. This process is very quick (typically one second).

2. Programming the SPI flash memory using Boundary Scan.

Once the SPI Flash memory has been programmed, the Spartan-3A device will automatically load from the Flash memory at power up. Generation of suitable Flash memory files (.mcs) can be achieved using ISE iMPACT's Prom File Formatter. This method of programming the SPI flash cannot be used on earlier versions of iMPACT (e.g.9.2) and you should use the method described in section3.

Right click on the icon representing the Spartan-3A and choose 'Add SPI/BPI Flash' Navigate to your programming file (.mcs) and click OPEN. Use the next dialogue box to select SPI flash and M25P128. Data width should be set to 1. The flash memory should appear as shown below.

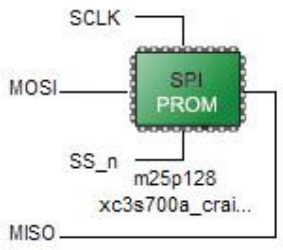


Right click on the icon representing the flash memory and choose 'Program' to load your program into the device. It is recommended that options to 'Verify' and 'Erase before programming' are

chosen. Otherwise all defaults can be accepted. The programming operation will take some time (at least 3 or 4 minutes)

3. Programming the SPI flash memory using Direct SPI Configuration.

This option is not available in versions of ISE iMPACT later than 11.5.
In the 'iMPACT Flows' window of the iMPACT Interface choose 'Direct SPI'. Right Click in the main window and choose 'Add SPI device'. Navigate to your Navigate to your programming file (.mcs) and click OPEN. Use the next dialogue box to select SPI flash and M25P128. Data width should be set to 1. The flash memory should appear as shown below.



Right click on the icon representing the flash memory and choose 'Program' to load your program into the device. It is recommended that options to 'Verify' and 'Erase before programming' are chosen. Otherwise all defaults can be accepted. The programming operation will take some time (at least 5 minutes).
Please note that to allow the FPGA to configure from the SPI Flash memory device you may need to remove the programming cable from the Craignell programming adapter.

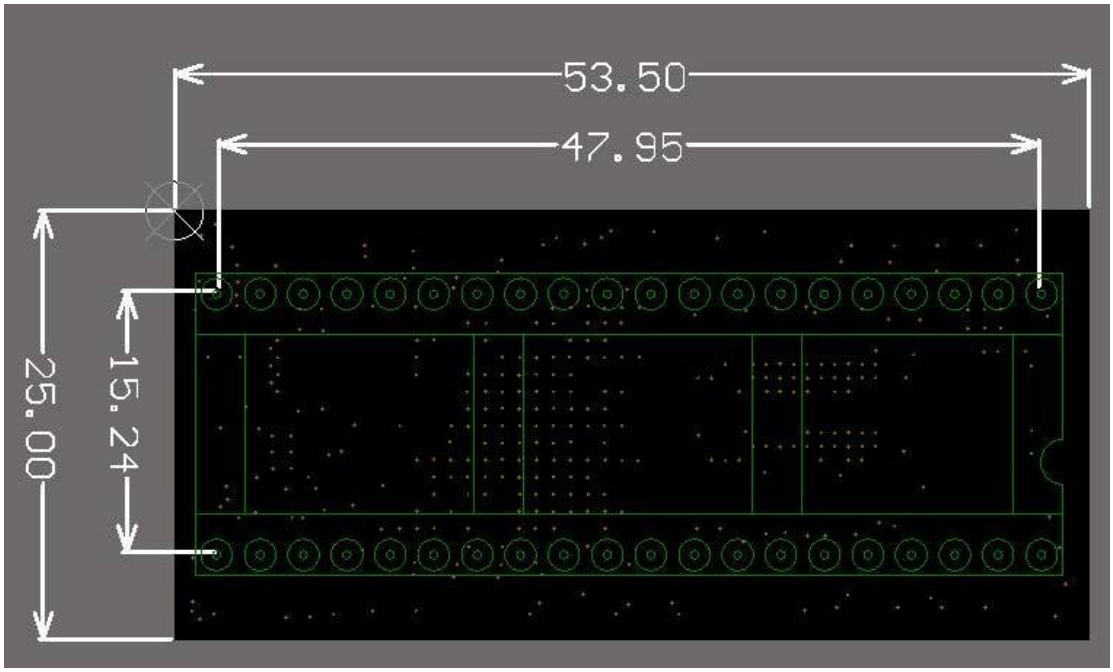
Pinout Constraints file

Pinout Constraints files (.ucf) for CR2-40 and CR2-48 can be found on the Enterpoint website at http://www.enterpoint.co.uk/component_replacements/craignell2.html.

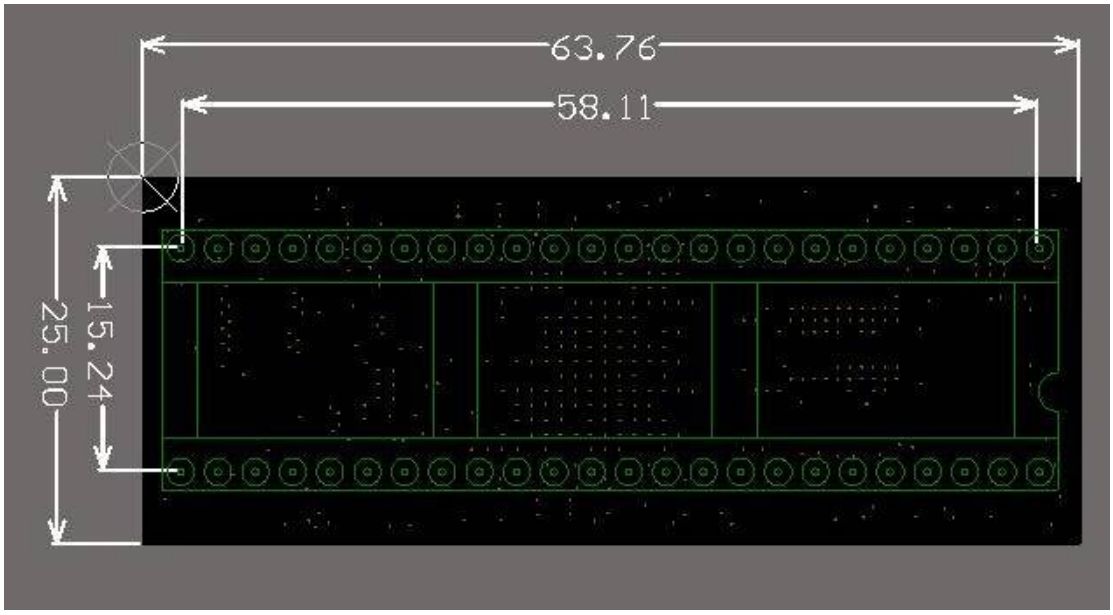
Mechanical Information

Dimensions are shown in Millimetres. The approximate overall height of Craignell2-40 and Craignell 2-48 is 16mm.

CR2-40



CR2-48



Medical and Safety Critical Use

Craignell2 boards are not authorised for the use in, or use in the design of, medical or other safety critical systems without the express written person of the Board of Enterpoint. If such use is allowed the said use will be entirely the responsibility of the user. Enterpoint Ltd will accept no liability for any failure or defect of the Craignell2 board, or its design, when it is used in any medical or safety critical application.

Warranty

Craignell2 comes with a 90 day return to base warranty.

Other specialised warranty programs can be offered to users of multiple Enterpoint products. Please contact sales on boardsales@enterpoint.co.uk if you are interested in these types of warranty,

Support

Enterpoint offers support during normal United Kingdom working hours 9.00am to 5.00pm. Please examine our Craignell2 FAQ web page and the contents of this manual before raising a support query. We can be contacted as follows:

Telephone - +44 (0) 1684 585262
Email - support@enterpoint.co.uk