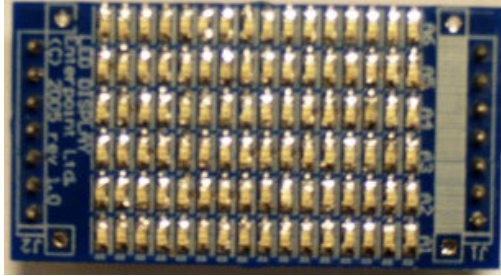




LED DISPLAY module, (Rev1.0)



This document will give a brief description of our LED DISPLAY module, this module has been designed to work on all of our development boards.

FEATURES:

- 96 Bright Red LED's arranged in a 6 by 16 array,
- Easy use implementing a scan technique,
- Power Track connections to provide power to lower modules,
- 4:16 Multiplexer for even easier operation.
- 1 in 16 resolution reliable visualization at 16MHz i.e. 1MHz per strip.

To initiate the LED DISPLAY it needs to be inserted in the development board host correctly this is achieved by ensuring that the power pins on the module are inserted in the host systems power structure i.e. at the very top of the socket header.

If the top of the socket is populated with one of our modules that supports the power track system then the power can be connected down to the module through the first one.

(Caution if implemented in this way make sure the FPGA does not drive the relevant pins on the development board host where the power pins are inserted.)

Once inserted in to the host system the user can begin to implement the scan, to light up the LED or LED's they wish, using the four inputs A0, A1, A2 and A3 are used to determine which of the 16 rows has the 6 LED's cathode switched to ground with all the rest set high to 3.3V.

With this in mind the user can then turn on which LED they wish by asserting the relevant pin high and turning the rest low, this can then be implement for each of the 16 rows individually to create the intended design.

Please see the relevant data sheet for the multiplexer CD74HC(T)154.

Also initiated on the module is the enable signals to turn the display of please seen relevant material.

Signal Table definition.

I N P U T S	nE1	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	
	nE2	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H
	A3	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	X	X	X
	A2	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H	H	X	X	X
	A1	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	H	X	X	X
	A0	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	H	X	X	X
O U T P U T S	nY0	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
	nY1	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
	nY2	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
	nY3	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
	nY4	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
	nY5	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
	nY6	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
	nY7	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	nY8	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	nY9	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	nY10	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
	nY11	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
	nY12	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
	nY13	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
	nY14	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
nY15	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	

H = Logic high.

L = Logic low.

X = Don't care.

n = Not (prefaces the signal to be inverted.)

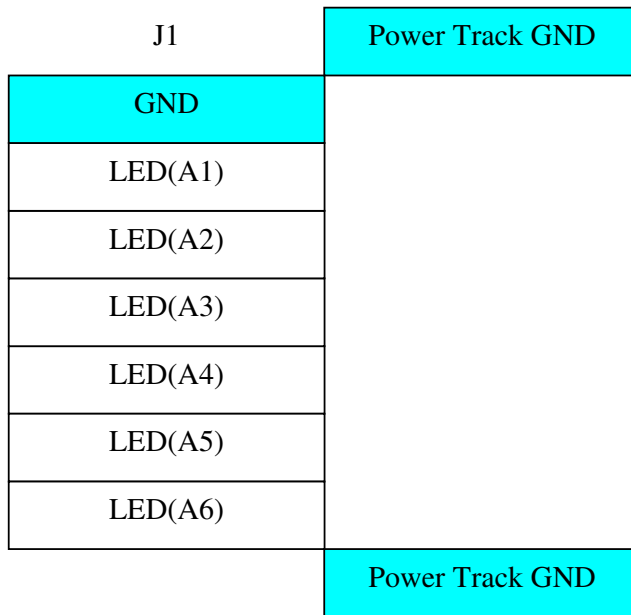


Figure 1: Pin out of J1.

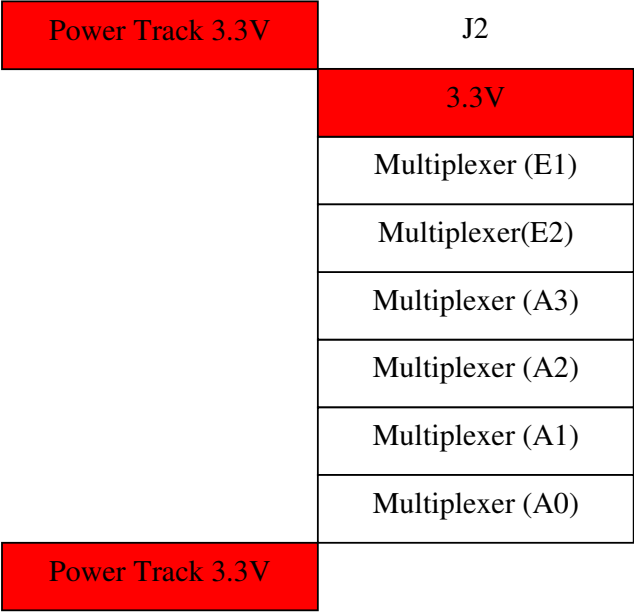


Figure 2: Pin out of J2.