



# Hollybush2 User Manual

Issue – 1.00

## **Kit Contents**

You should receive the following items with you Hollybush1 development kit:

1 – Hollybush2 Board

## **Optional Programming Accessories**

PROG2 Programming Cable  
Hollybush2 Programming Adapter  
PROG3 Programming Cable

## **Foreword**

**PLEASE READ THIS ENTIRE MANUAL BEFORE PLUGGING IN  
OR POWERING UP YOUR HOLLYBUSH2 BOARD.  
PLEASE TAKE SPECIAL NOTE OF THE WARNINGS WITHIN  
THIS MANUAL.**

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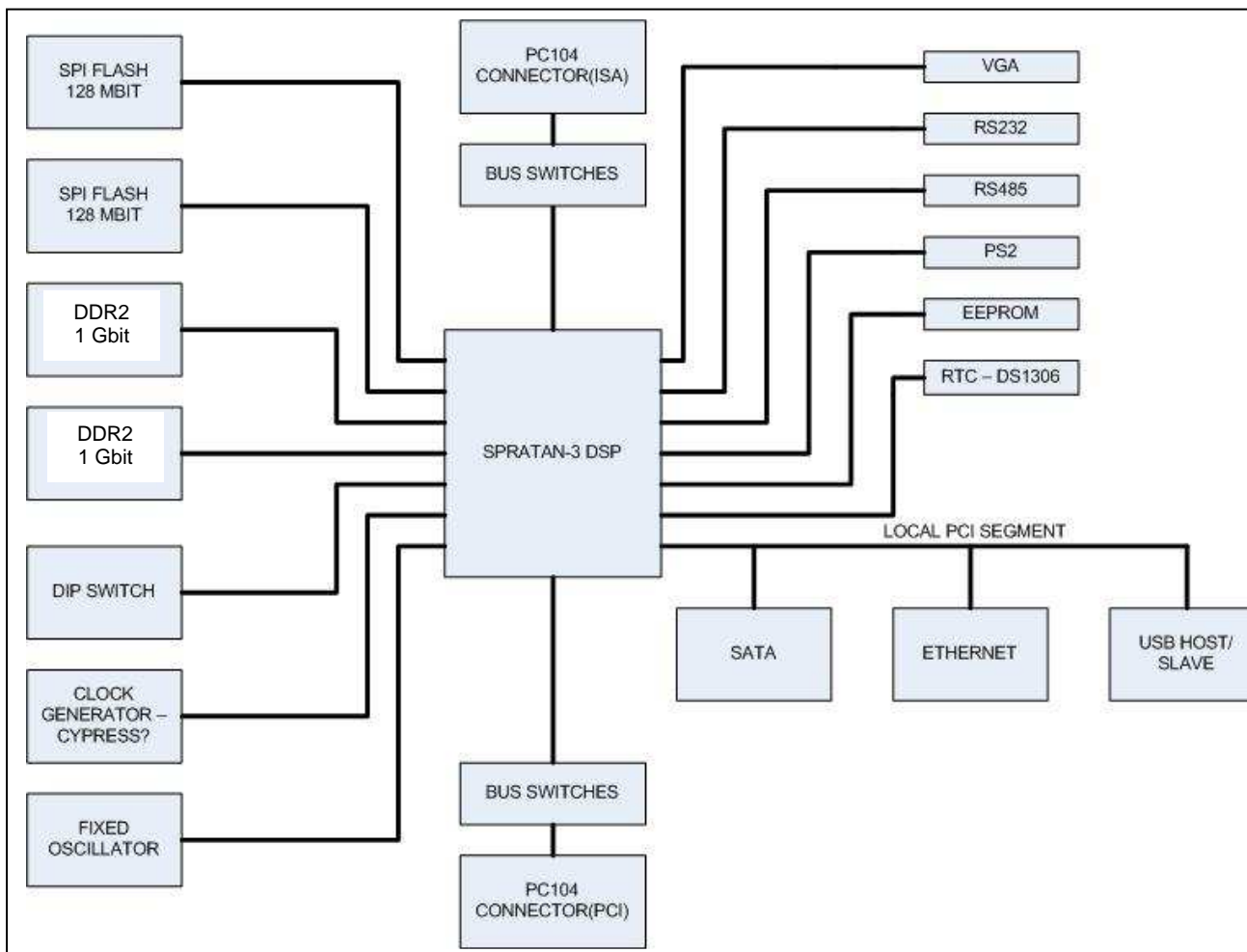
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## Introduction

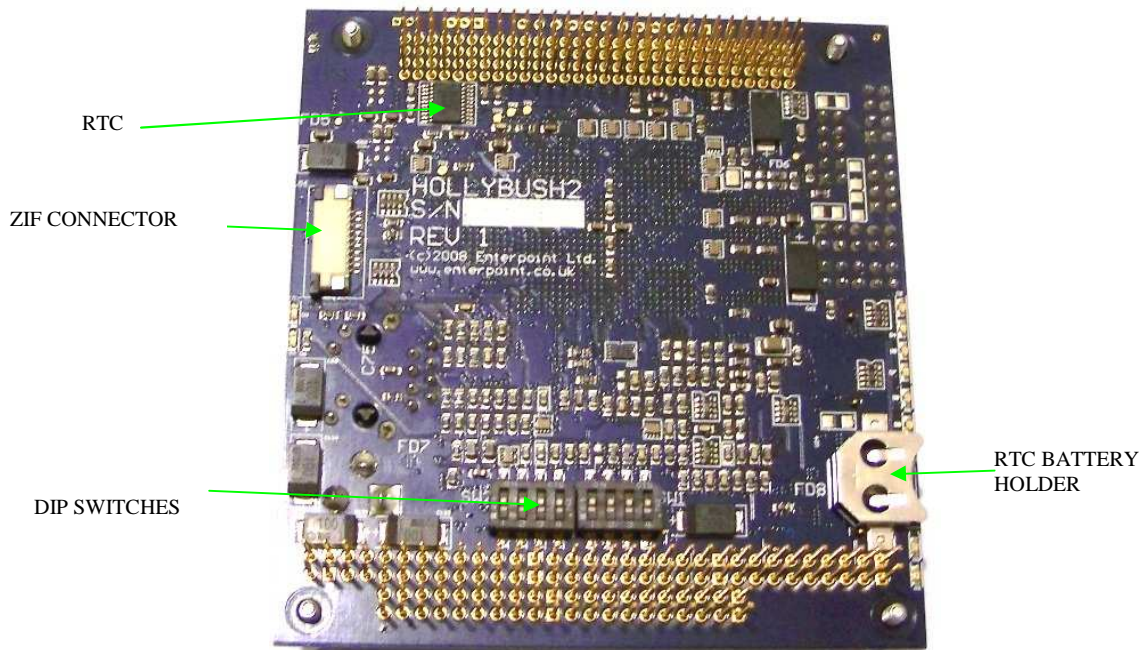
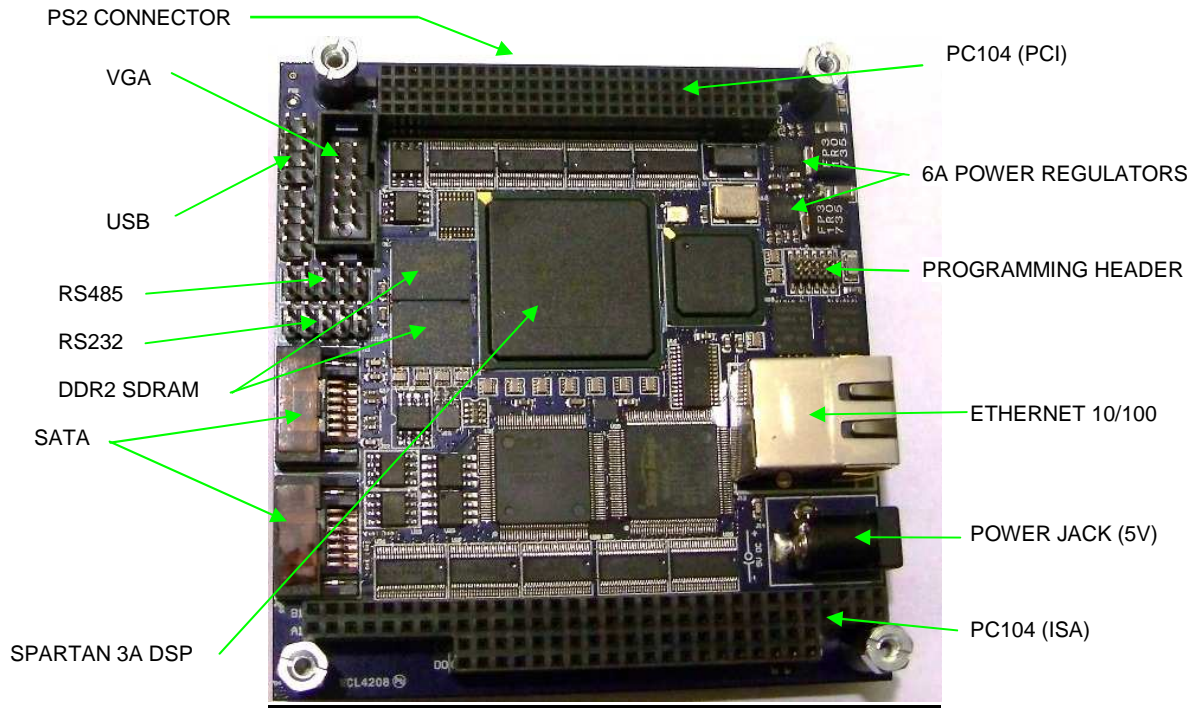
Welcome to your Hollybush2 board. Hollybush2 is a highly featured Spartan™-3A DSP FPGA based PC104/PC104+ processor board.

The aim of this manual is to assist in using the main features of Hollybush2. Should this manual fail to explain a feature sufficiently then our support team can be reached by email on [support@enterpoint.co.uk](mailto:support@enterpoint.co.uk).



**Hollybush2 Function Block Diagram**

## Finding Your Way Around



## **Getting Started**

Ensure that any vital data, contained within your host system, is backed up before attempting to use your Hollybush2 in any hosting system.

Your Hollybush2 normally comes in an un-programmed state so the PC104 interfaces will not operate. These interfaces will need the Spartan<sup>TM</sup>3A DSP to be configured with a design for these to operate in the normal way as PC104 interfaces. Enterpoint can supply ISA and PCI cores at extra cost if these are required.

## **Hollybush2 Main Features**

Hollybush2 has many possible modes of operation and many possible uses in systems. Envisaged applications include one or more of the following:

1. Hosting Processor Board (MicroBlaze™, 8086, Z80 or other soft IP processors implemented within FPGA)
2. DSP High Performance Engine.
3. Coprocessor Engine for biometric processing and financial modelling.
4. Processor Arrays.
5. ISA to PCI Bridge.
6. PCI to ISA Bridge.

The feature set supplied on the Hollybush2 is aimed at providing a complete processor solution for the embedded marketplace. The rugged PC104 Plus format enables use in challenging environments.

Hollybush2 can be stacked with other PC104 boards of either ISA or PCI varieties.

Hollybush2 can operate from a single 5V power input. This can be supplied through a 2.1mm jack or through either of the PC104 connectors.

Complimentary products including a 12-48V DC power supply will be available shortly.

## **FPGA**

The heart of the Hollybush2 is a Xilinx XC3SD3400A Spartan3A-DSP FPGA. This device offers approximately 3.4M gates of logic capability with substantial numbers of DSP48A and SRAM blocks available as processing resource.

Hollybush2 supports one Spartan-3A 3400 device in the FG676 package. Standard builds of Hollybush2 use commercial grade devices but industrial grade parts can be fitted at extra cost.

## **FPGA JTAG and Configuration**

Hollybush2 uses a compact 6x2 1.27mm header to provide an interface for both JTAG and SPI Flash direct programming.

An adapter from the compact header to 2x7 2mm headers (Xilinx™ standard) is available.

Xilinx™ ISE™ tools can be used as programming software.

Our Parallel port programming cable Prog2 or our USB programming cable Prog3 can be used as a programming lead.

When used as a JTAG interface this connector has a JTAG chain consisting of a single device the XC3SD3400A.

The primary SPI Flash contains the configuration data for the FPGA. The primary SPI Flash is 128Mbits in size. Only about 12Mbits are necessary to configure the XC3SD3400A with a single bitstream. The balance of the SPI Flash can be used for multiple bitstreams and /or data or code storage.

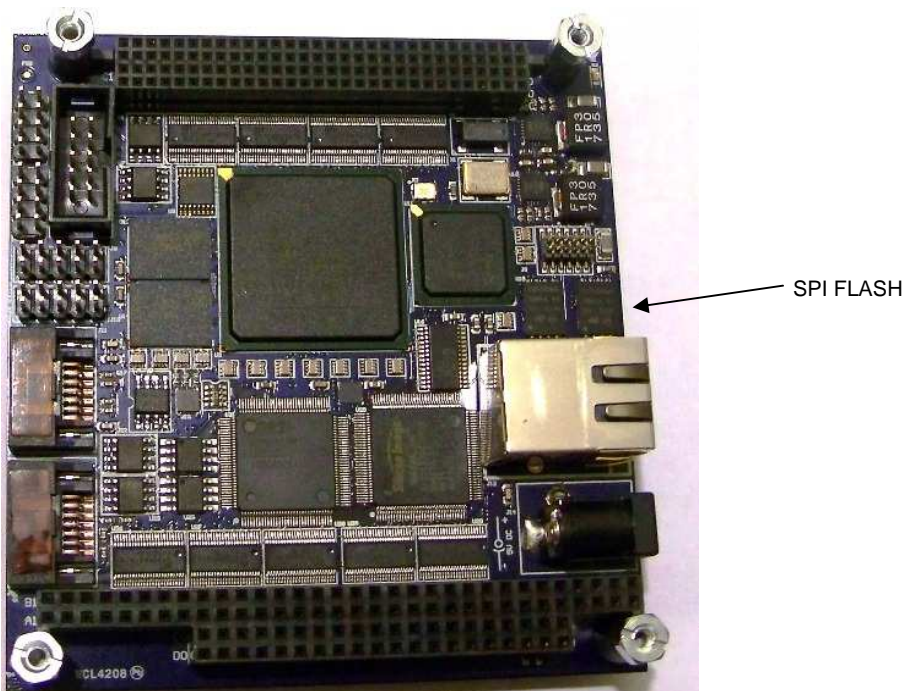
When the 6x2 header is used for SPI Flash programming this interface will only program the primary SPI Flash. The secondary SPI Flash programming is not supported by this interface and will need logic implementation with the FPGA to affect programming.

Indirect programming of the primary SPI Flash is also possible using JTAG mode. This will need ISE™ version 9.2 or later for this mode of operation.

## SPI Flash

Hollybush2 has two 128 Mbit M25P128 SPI Flash memories. The primary SPI Flash is used for the FPGA configuration as previously described. The secondary SPI is totally unallocated and can be used as microprocessor code and data storage such as for a MicroBlaze™ processor. The connections between the secondary SPI Flash memory and the FPGA are shown below:

| M25P128 function | M25P128 Pin | FPGA Pin |
|------------------|-------------|----------|
| #S               | 1           | L22      |
| Q                | 2           | L23      |
| D                | 5           | L20      |
| C                | 6           | L18      |



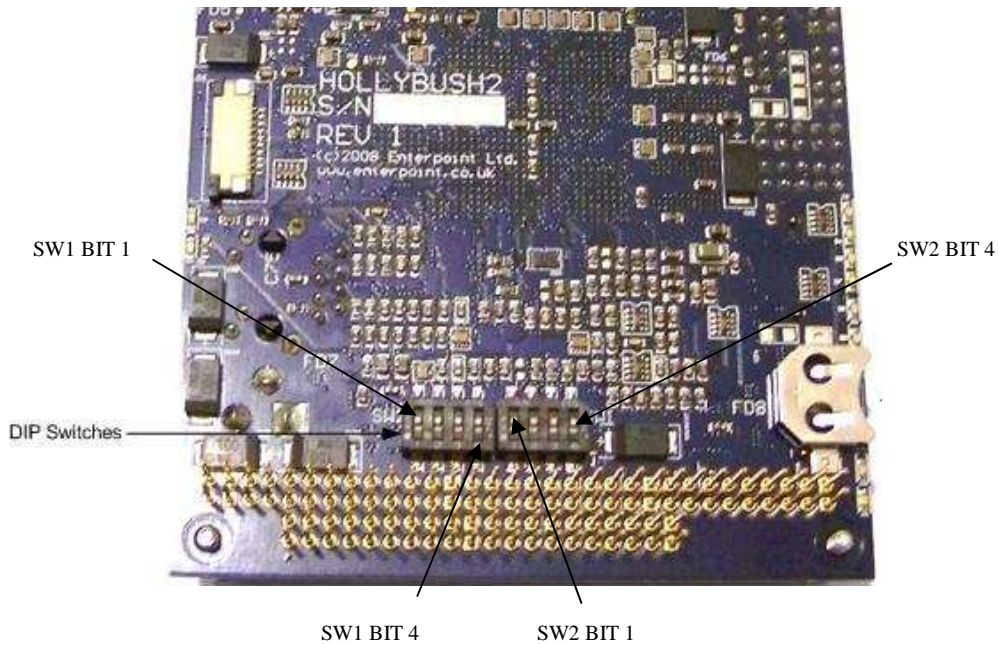
## **DDR2 DRAM**

Hollybush2 has one DDR2 bank consisting of 2 devices (DDR\_A and DDR\_B). The memory devices used are MT47H32M16 or a similar alternative. The address and control lines are shared so that the devices operate as a single x32 memory bank. The pin assignments are shown below:

| <b>DDR Function</b> | <b>DDR Pin</b> | <b>FPGA</b> | <b>DDR Function</b> | <b>DDR Pin</b> | <b>FPGA</b> |
|---------------------|----------------|-------------|---------------------|----------------|-------------|
| DQ0 (DDR_A)         | G8             | Y6          | A0                  | M8             | K3          |
| DQ1 (DDR_A)         | G2             | V8          | A1                  | M3             | L3          |
| DQ2 (DDR_A)         | H7             | AB1         | A2                  | M7             | L4          |
| DQ3 (DDR_A)         | H3             | AC1         | A3                  | N2             | M7          |
| DQ4 (DDR_A)         | H1             | Y5          | A4                  | N8             | M8          |
| DQ5 (DDR_A)         | H9             | U9          | A5                  | N3             | M3          |
| DQ6 (DDR_A)         | F1             | U7          | A6                  | N7             | M4          |
| DQ7 (DDR_A)         | F9             | U8          | A7                  | P2             | M6          |
| DQ8 (DDR_A)         | C8             | AA2         | A8                  | P8             | M5          |
| DQ9 (DDR_A)         | C2             | T7          | A9                  | P3             | N4          |
| DQ10 (DDR_A)        | D7             | Y1          | A10                 | M2             | N5          |
| DQ11 (DDR_A)        | D3             | Y2          | A11                 | P7             | N2          |
| DQ12 (DDR_A)        | D1             | U6          | A12                 | R2             | N1          |
| DQ13 (DDR_A)        | D9             | AA3         | A13                 | R8             | N7          |
| DQ14 (DDR_A)        | B1             | U5          | A14                 | R3             | M1          |
| DQ15 (DDR_A)        | B9             | V5          | A15                 | R7             | M2          |
| DQ16 (DDR_B)        | G8             | V1          | UDQS (DDR_A)        | B7             | W3          |
| DQ17 (DDR_B)        | G2             | R5          | #UDQS (DDR_A)       | A8             | W4          |
| DQ18 (DDR_B)        | H7             | R8          | LDQS (DDR_A)        | F7             | V7          |
| DQ19 (DDR_B)        | H3             | U2          | #LDQS (DDR_A)       | E8             | V6          |
| DQ20 (DDR_B)        | H1             | P8          | UDQS (DDR_B)        | B7             | R3          |
| DQ21 (DDR_B)        | H9             | P9          | #UDQS (DDR_B)       | A8             | R4          |
| DQ22 (DDR_B)        | F1             | R7          | LDQS (DDR_B)        | F7             | T5          |
| DQ23 (DDR_B)        | F9             | R6          | #LDQS (DDR_B)       | E8             | U4          |
| DQ24 (DDR_B)        | C8             | R2          | ODT                 | K9             | K6          |
| DQ25 (DDR_B)        | C2             | P7          | LDM (DDR_A)         | F3             | V2          |
| DQ26 (DDR_B)        | D7             | P3          | UDM (DDR_A)         | B3             | U1          |
| DQ27 (DDR_B)        | D3             | T4          | LDM (DDR_B)         | F3             | P10         |
| DQ28 (DDR_B)        | D1             | P6          | UDM (DDR_B)         | B3             | N6          |
| DQ29 (DDR_B)        | D9             | T3          | BA0                 | L2             | K5          |
| DQ30 (DDR_B)        | B1             | N9          | BA1                 | L3             | K2          |
| DQ31 (DDR_B)        | B9             | P4          | CKE                 | K2             | K4          |
| #CS                 | L8             | M10         | CLK (DDR_A)         | J8             | AD1         |
| #RAS                | K7             | M9          | #CLK (DDR_A)        | K8             | AD2         |
| #CAS                | L7             | J5          | CLK (DDR_B)         | J8             | AC2         |
| #WE                 | K3             | J4          | #CLK (DDR_B)        | K8             | AC3         |
| DQS_LOOP_IN         | NONE           | T9          | DQS_LOOP_OUT        | NONE           | T10         |
| #DDR_RESET_IN       | NONE           | H2          |                     |                |             |

## DIP Switches

There are two 4 bit DIP switches available, SW1 and SW2. These are mounted on the underside of the PCB.



| SWITCH | BIT | FPGA PIN | SWITCH | ELEMENT | FPGA PIN |
|--------|-----|----------|--------|---------|----------|
| 1      | 1   | V26      | 2      | 1       | P21      |
| 1      | 2   | U26      | 2      | 2       | N23      |
| 1      | 3   | R24      | 2      | 3       | N25      |
| 1      | 4   | R23      | 2      | 4       | N26      |

## **Clocks**

There is a 7x5mm fixed oscillator on Hollybush2 of normally 32 MHz. It is connected to pin J14 of the FPGA.

The Real Time Clock 32.768KHz output is connected to the FPGA at pin C18.

There is also a Cypress CY22394 clock generator capable of generating three single ended clocks and one differential clock which all which are connected to FPGA. The clock generator is controlled by SPI interface. The connections between the Clock Generator and the FPGA are shown below:

| <b>CY22394 Function</b>         | <b>CY22394FXI Pin</b> | <b>FPGA Pin</b> |
|---------------------------------|-----------------------|-----------------|
| CLK C                           | 1                     | B14             |
| P-CLK (Differential Clock -ve)  | 7                     | V11             |
| P+ CLK (Differential Clock +ve) | 8                     | U11             |
| CLKB                            | 9                     | B13             |
| CLKA                            | 10                    | C13             |
| SDAT                            | 12                    | AE26            |
| SCLK                            | 13                    | C17             |
| S2/SUSPEND                      | 15                    | F17             |
| SHUTDOWN/OE                     | 16                    | C23             |

There is also a 25MHz oscillator. It is connected to the Ethernet and SATA controller only.

## **PC104 Interface**

Hollybush2 supports both ISA and PCI connectors of the PC104+ standard. FPGA IP to control these interfaces is necessary for either or both to operate. Enterpoint can supply ISA and PCI FPGA cores at extra cost. Either or both of these interfaces can be used in non-standard ways when not used as PC104 standard interfaces, for example as low latency links or even star connections using LVDS. These structures can be advantageous in systems where bus negotiation could cause latency issues.

Hollybush2 can act as a master or slave card on either ISA, or PCI PC104 interfaces. Use and mode of the ISA interface is normally independent of the PCI interface. Similarly the PCI interface can be used totally independently of the ISA interface. It is also possible to operate these interfaces in a bridge function between ISA and PCI and in either direction subject to suitable IP implementation in the FPGA design.

The signals on both the PC104 interfaces are connected to the FPGA via bus switches.

The location of pins A1, B1, C1 and D1 are marked on the board near the PCI 104 connector (4x30 way) as are the locations of pins A1, B1, C0, D0, A32, B32, C19 and D19 of the PC104 connector.

### ISA connections:

|     |      |     |      |     |      |     |      |
|-----|------|-----|------|-----|------|-----|------|
| B1  | DGND | A1  | AE3  |     |      |     |      |
| B2  | AF3  | A2  | AE4  |     |      |     |      |
| B3  | VD5V | A3  | AF4  |     |      |     |      |
| B4  | AF5  | A4  | AD6  |     |      |     |      |
| B5  | NC   | A5  | AC6  |     |      |     |      |
| B6  | AE6  | A6  | AD7  |     |      |     |      |
| B7  | NC   | A7  | AB7  |     |      |     |      |
| B8  | AD11 | A8  | AC8  |     |      |     |      |
| B9  | NC   | A9  | AE7  | C0  | DGND | D0  | DGND |
| B10 | AF8  | A10 | AB9  | C1  | AE8  | D1  | Y9   |
| B11 | W10  | A11 | W9   | C2  | Y10  | D2  | AC9  |
| B12 | AB12 | A12 | Y12  | C3  | AC12 | D3  | V10  |
| B13 | AF13 | A13 | AE13 | C4  | AF12 | D4  | W13  |
| B14 | AA13 | A14 | W12  | C5  | V13  | D5  | AE12 |
| B15 | Y13  | A15 | AF14 | C6  | Y14  | D6  | V14  |
| B16 | AC14 | A16 | AD15 | C7  | AD14 | D7  | AE14 |
| B17 | Y15  | A17 | W15  | C8  | AC15 | D8  | AE15 |
| B18 | V16  | A18 | U16  | C9  | U15  | D9  | V15  |
| B19 | AE17 | A19 | V17  | C10 | AC16 | D10 | AB16 |
| B20 | AB18 | A20 | AF18 | C11 | Y20  | D11 | W17  |
| B21 | AC20 | A21 | AF19 | C12 | AE19 | D12 | AE18 |
| B22 | AA17 | A22 | AD21 | C13 | AD20 | D13 | AE20 |

|     |      |     |      |     |      |     |      |
|-----|------|-----|------|-----|------|-----|------|
| B23 | AB23 | A23 | AA22 | C14 | AC19 | D14 | Y17  |
| B24 | AC21 | A24 | AF20 | C15 | AD19 | D15 | AF23 |
| B25 | AD22 | A25 | AC22 | C16 | AE21 | D16 | VD5V |
| B26 | AE23 | A26 | AD17 | C17 | AC23 | D17 | AA23 |
| B27 | AF25 | A27 | AB24 | C18 | AA24 | D18 | DGND |
| B28 | AA25 | A28 | AD25 | C19 | AE25 | D19 | DGND |
| B29 | VD5V | A29 | AD26 |     |      |     |      |
| B30 | Y25  | A30 | AC26 |     |      |     |      |
| B31 | DGND | A31 | AC25 |     |      |     |      |
| B32 | DGND | A32 | DGND |     |      |     |      |

### PCI Connections:

|     |       |     |       |     |       |     |       |
|-----|-------|-----|-------|-----|-------|-----|-------|
| A1  | DGND  | B1  | NC    | C1  | VD5V  | D1  | C7    |
| A2  | VIO   | B2  | J16   | C2  | C5    | D2  | VD5V  |
| A3  | F7    | B3  | DGND  | C3  | C6    | D3  | D6    |
| A4  | G8    | B4  | E7    | C4  | DGND  | D4  | B2    |
| A5  | DGND  | B5  | H9    | C5  | F8    | D5  | DGND  |
| A6  | D9    | B6  | VIO   | C6  | D8    | D6  | G9    |
| A7  | D10   | B7  | E10   | C7  | DGND  | D7  | G10   |
| A8  | VD3V3 | B8  | A4    | C8  | F12   | D8  | VD3V3 |
| A9  | C11   | B9  | DGND  | C9  | NC    | D9  | C8    |
| A10 | DGND  | B10 | A9    | C10 | VD3V3 | D10 | NC    |
| A11 | H10   | B11 | VD3V3 | C11 | K11   | D11 | DGND  |
| A12 | VD3V3 | B12 | F14   | C12 | DGND  | D12 | K12   |
| A13 | J11   | B13 | DGND  | C13 | F15   | D13 | VD3V3 |
| A14 | DGND  | B14 | F13   | C14 | VD3V3 | D14 | C12   |
| A15 | G12   | B15 | VD3V3 | C15 | J12   | D15 | DGND  |
| A16 | A14   | B16 | H12   | C16 | DGND  | D16 | D13   |
| A17 | VD3V3 | B17 | C15   | C17 | E14   | D17 | VD3V3 |
| A18 | D16   | B18 | DGND  | C18 | C16   | D18 | G15   |
| A19 | F19   | B19 | J20   | C19 | VIO   | D19 | D17   |
| A20 | DGND  | B20 | F20   | C20 | E17   | D20 | DGND  |
| A21 | C21   | B21 | VD5V  | C21 | D20   | D21 | C20   |
| A22 | VD5V  | B22 | E21   | C22 | DGND  | D22 | G17   |
| A23 | G20   | B23 | DGND  | C23 | D21   | D23 | VIO   |
| A24 | DGND  | B24 | D22   | C24 | VD5V  | D24 | C22   |
| A25 | F22   | B25 | VIO   | C25 | G21   | D25 | DGND  |
| A26 | VD5V  | B26 | C25   | C26 | DGND  | D26 | D23   |
| A27 | C26   | B27 | VD5V  | C27 | J22   | D27 | DGND  |
| A28 | DGND  | B28 | F23   | C28 | VD5V  | D28 | G22   |
| A29 | NC    | B29 | F24   | C29 | G23   | D29 | D26   |
| A30 | NC    | B30 | F25   | C30 | G24   | D30 | DGND  |

## Local PCI

A local PCI segment wires SATA, Ethernet and USB Host controllers. The FPGA with a suitable PCI core acts as master and arbiter to this internal PCI segment. The connections to the FPGA are shown below:

| Signal Name | FPGA pin | ISP1561BM pin | SIL3512ECTU128 pin | LU82551ER pin |
|-------------|----------|---------------|--------------------|---------------|
| AD0         | W21      | 84            | 1                  | N7            |
| AD1         | Y21      | 82            | 128                | M7            |
| AD2         | Y24      | 81            | 127                | P6            |
| AD3         | Y23      | 79            | 126                | P5            |
| AD4         | V25      | 78            | 125                | N5            |
| AD5         | AA14     | 77            | 124                | M5            |
| AD6         | AA18     | 75            | 121                | P4            |
| AD7         | V22      | 74            | 120                | N4            |
| AD8         | V18      | 71            | 118                | P3            |
| AD9         | V19      | 70            | 117                | N3            |
| AD10        | V21      | 68            | 115                | N2            |
| AD11        | U21      | 67            | 114                | M1            |
| AD12        | W20      | 66            | 111                | M2            |
| AD13        | U18      | 64            | 110                | M3            |
| AD14        | U23      | 63            | 109                | L1            |
| AD15        | V24      | 62            | 108                | L2            |
| AD16        | T24      | 46            | 95                 | K1            |
| AD17        | M18      | 44            | 94                 | E3            |
| AD18        | M26      | 43            | 93                 | D1            |
| AD19        | L17      | 42            | 90                 | D2            |
| AD20        | K26      | 40            | 89                 | D3            |
| AD21        | M21      | 39            | 88                 | C1            |
| AD22        | K21      | 38            | 87                 | B1            |
| AD23        | J23      | 36            | 86                 | B2            |
| AD24        | N21      | 32            | 83                 | B4            |
| AD25        | P20      | 31            | 82                 | A5            |
| AD26        | N24      | 30            | 79                 | B5            |
| AD27        | R25      | 28            | 78                 | B6            |
| AD28        | P23      | 27            | 77                 | C6            |
| AD29        | P25      | 26            | 74                 | C7            |
| AD30        | K22      | 24            | 73                 | A8            |
| AD31        | K20      | 23            | 72                 | B8            |
| CBE0        | W23      | 72            | 119                | M4            |
| CBE1        | U20      | 60            | 105                | L3            |
| CBE2        | M25      | 47            | 96                 | F3            |
| CBE3        | L24      | 34            | 84                 | C4            |
| PAR         | T20      | 59            | 104                | J1            |
| SERR        | M24      | 58            | 103                | A2            |
| PERR        | U22      | 56            | 99                 | J2            |
| STOP        | V23      | 54            | 100                | H1            |
| DEVSEL      | U19      | 52            | 101                | H3            |

|        |     |    |     |    |
|--------|-----|----|-----|----|
| TRDY   | T17 | 51 | 102 | G3 |
| IRDY   | T18 | 50 | 98  | F1 |
| FRAME  | Y22 | 48 | 97  | F2 |
| IDSEL0 | K25 |    |     | A4 |
| IDSEL1 | U24 |    | 85  |    |
| IDSEL2 | M22 | 35 |     |    |
| REQ0   | M19 |    |     | C3 |
| REQ1   | R19 |    | 72  |    |
| REQ2   | M20 | 22 |     |    |
| GNT0   | R26 |    |     | J3 |
| GNT1   | R22 |    | 70  |    |
| GNT2   | M23 | 20 |     |    |
| RST    | N19 | 18 | 68  | C2 |
| INTA0  | P26 |    |     | H2 |
| INTA1  | R18 |    | 67  |    |
| INTA2  | K19 | 16 |     |    |
| CLK    | N18 | 19 | 69  | G1 |

## SATA Interface

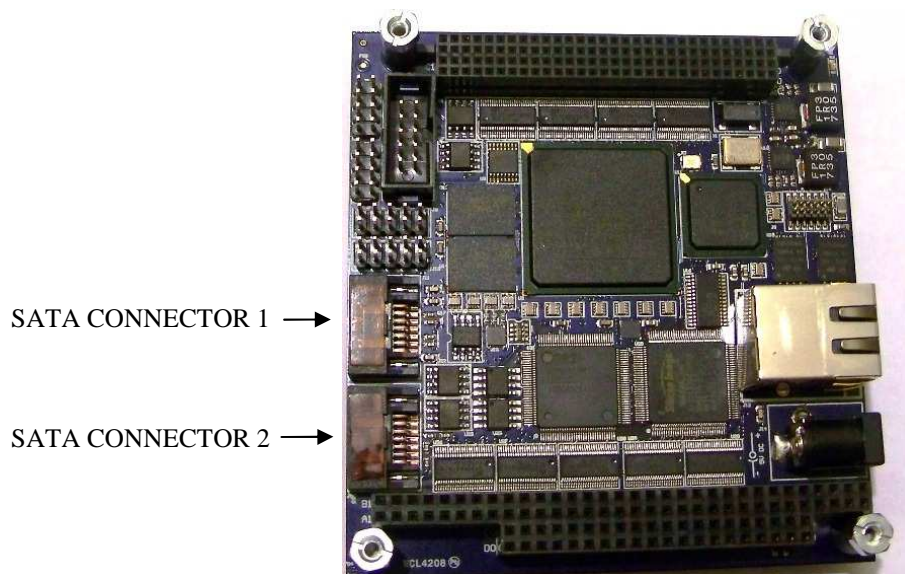
Hollybush2 implements a twin SATA interface using a Silicon Image SIL3512. This chip is connected to the FPGA over a local PCI bus within Hollybush2. To make full use of this interface will require a PCI core implementation within the FPGA design. The pin assignments between the SIL3512 and the FPGA are shown above (see 'Local PCI').

The SIL3512 is capable of supporting SATA-I interfaces.

The connections between the SATA connectors and the SIL3512 device are shown below:

| SATA CONNECTORS |     |        | SIL3512 |           |
|-----------------|-----|--------|---------|-----------|
| connector       | pin | signal | pin     | signal    |
| 1               | 2   | TXP1   | 20      | SATA_TXP1 |
| 1               | 3   | TXN1   | 19      | SATA_TXN1 |
| 1               | 5   | RXN1   | 15      | SATA_RXN1 |
| 1               | 6   | RXP1   | 14      | SATA_RXP1 |
| 2               | 2   | TXP2   | 11      | SATA_TXP2 |
| 2               | 3   | TXN2   | 10      | SATA_TXN2 |
| 2               | 5   | RXN2   | 6       | SATA_RXN2 |
| 2               | 6   | RXP2   | 5       | SATA_RXP2 |

The SATA pins not listed above are connected to DGND.



## **Ethernet Interface**

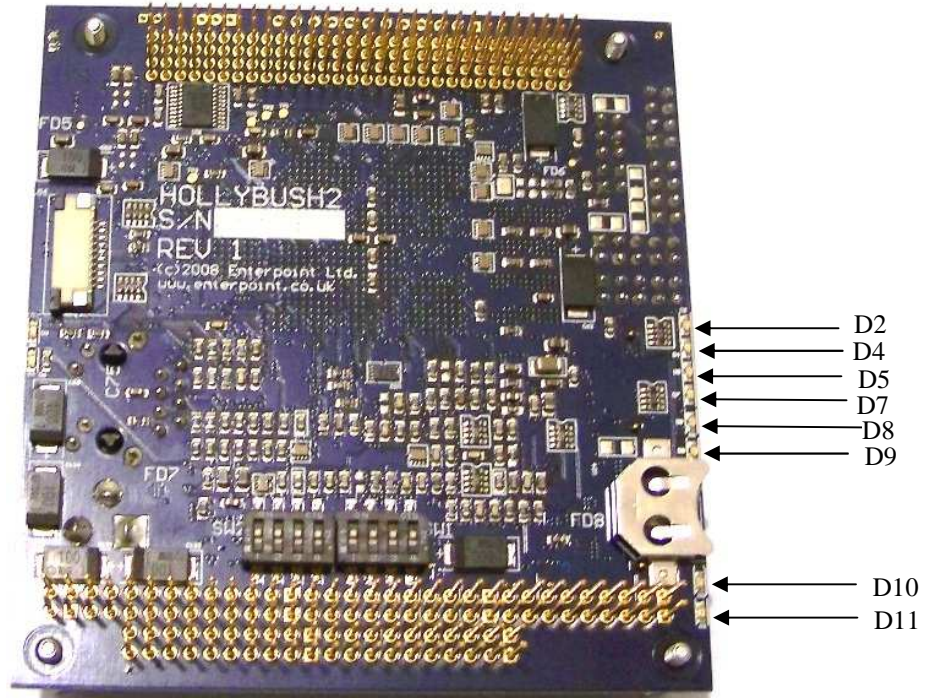
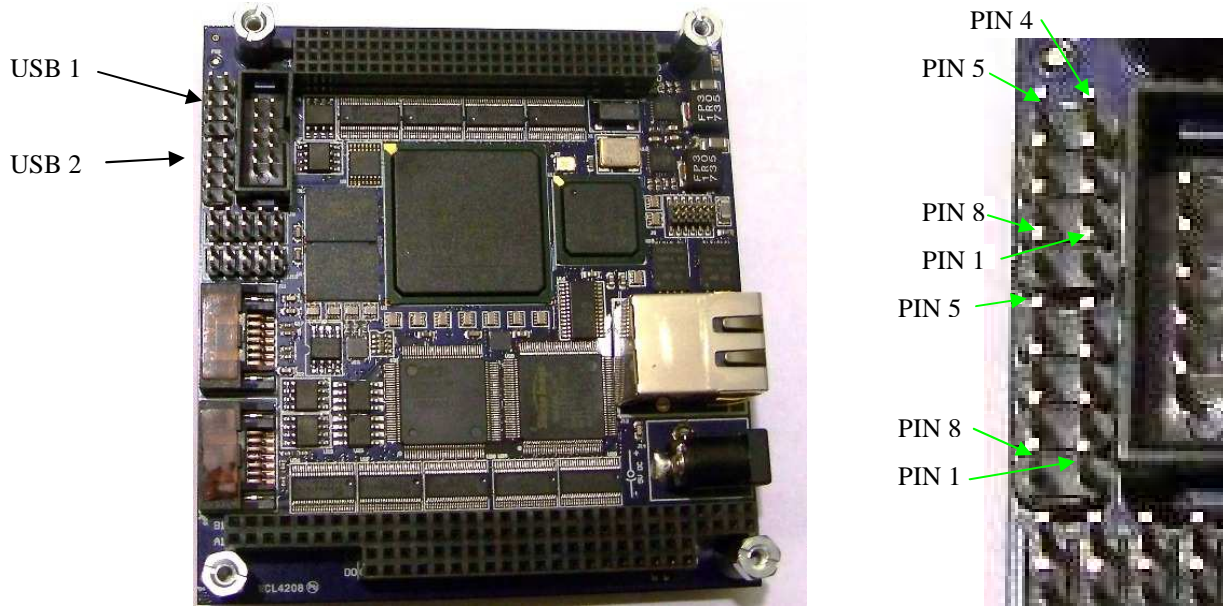
Hollybush2 has an Intel LU82551ER combined Ethernet MAC and PHY on board. This interface supports 10T/100T interfaces through an RJ45 jack. The LU82551ER is accessed through the local PCI segment and therefore needs a PCI core implementation within the FPGA. The pin assignments between the LU82551 and the FPGA are shown above (see 'Local PCI').

## **USB Host Interface**

A NXP ISP1561BM USB Host Controller supports two 480 Mbit/s interfaces. This controller is supported with MIC2026 power switches and controlled over the local PCI segment. Use of these interfaces will require the implementation of a PCI core within the FPGA design. The pin assignments between the ISP1561 and the FPGA are shown above (see 'Local PCI').

The USB signals are accessible on two 4 x 2 x 0.1inch headers. The connections between the ISP1561 and these headers are shown below. The presence of the output signals and 'Link present' signals are indicated by LEDs, also shown below :

| <b>Signal</b> | <b>Header</b> |   | <b>Isp1561</b> | <b>LED</b> |
|---------------|---------------|---|----------------|------------|
| OUT4/OC1      | USB1          | 1 | 89             | D2         |
| DP1           | USB 1         | 2 | 103            |            |
| DM1           | USB 1         | 3 | 102            |            |
| DM2           | USB 1         | 6 | 109            |            |
| DP2           | USB 1         | 7 | 110            |            |
| OUT3/OC2      | USB 1         | 8 | 96             | D5         |
| OUT2/OC3      | USB 2         | 1 | 105            | D8         |
| DP3           | USB 2         | 2 | 117            |            |
| DM3           | USB 2         | 3 | 116            |            |
| DM4           | USB 2         | 6 | 122            |            |
| DP4           | USB 2         | 7 | 123            |            |
| OUT1/OC4      | USB 2         | 8 | 119            | D10        |
| GL1           | -             | - | 91             | D4         |
| GL2           | -             | - | 98             | D7         |
| GL3           | -             | - | 112            | D9         |
| GL4           | -             | - | 125            | D11        |



## **Real Time Clock**

A Maxim (Dallas) DS1306 Real Time Clock chip provides a timekeeping facility on Hollybush2. It can be battery backed to maintain time when the Hollybush2 is unpowered. A battery holder is located on the back of the Hollybush2 and can support a CR1220 type battery. The RTC also has a small RAM area that can be used as a data store.

| <b>Signal</b> | <b>DS1306 Pin</b> | <b>FPGA PIN</b> |
|---------------|-------------------|-----------------|
| SDI           | 15                | B17             |
| #INT1         | 8                 | B21             |
| #INT0         | 7                 | B20             |
| 32KHZ         | 18                | C18             |
| SDO           | 16                | B18             |
| SCLK          | 14                | B19             |
| CE            | 12                | B15             |

## **EEprom**

A 16Kbit EEprom type 24C16 is available for data storage on Hollybush2.

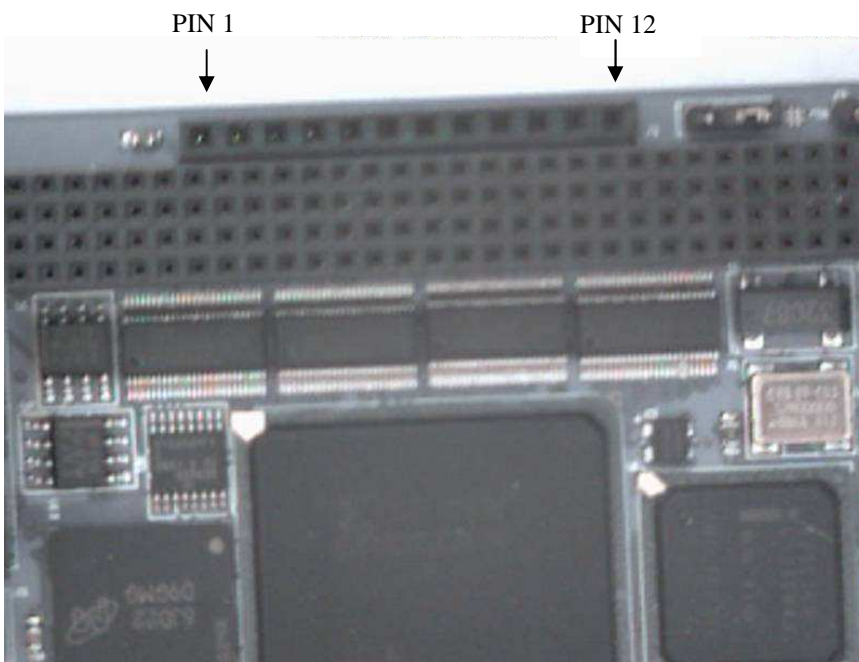
| <b>EEPROM PIN</b> | <b>FPGA PIN</b> |
|-------------------|-----------------|
| SDA               | D24             |
| SCL               | E26             |
| WP                | E24             |

## PS2 Interfaces

Hollybush2 supports a twin PS2 interface. It is available on a 12x1 connector and a break out cable to PS2 connectors is available at extra cost. It is also possible to use this interface as a general I/O port. The function and usage is entirely dependent on the FPGA design feature support. These signals connect to the FPGA via bus switches and are 5v tolerant.

| PS2 connector | FPGA PIN    |
|---------------|-------------|
| PIN 1         | E15         |
| PIN 2         | G13         |
| PIN 3         | Wired to 5V |
| PIN 4         | Wired to 0V |
| PIN 5         | B3          |
| PIN 6         | B4          |
| PIN 7         | D18         |
| PIN8          | K14         |
| PIN 9         | Wired to 5V |
| PIN 10        | Wired to 0V |
| PIN 11        | K16         |
| PIN 12        | H17         |

The PS2 connector is situated just above the 4x30 PCI connector as shown below:

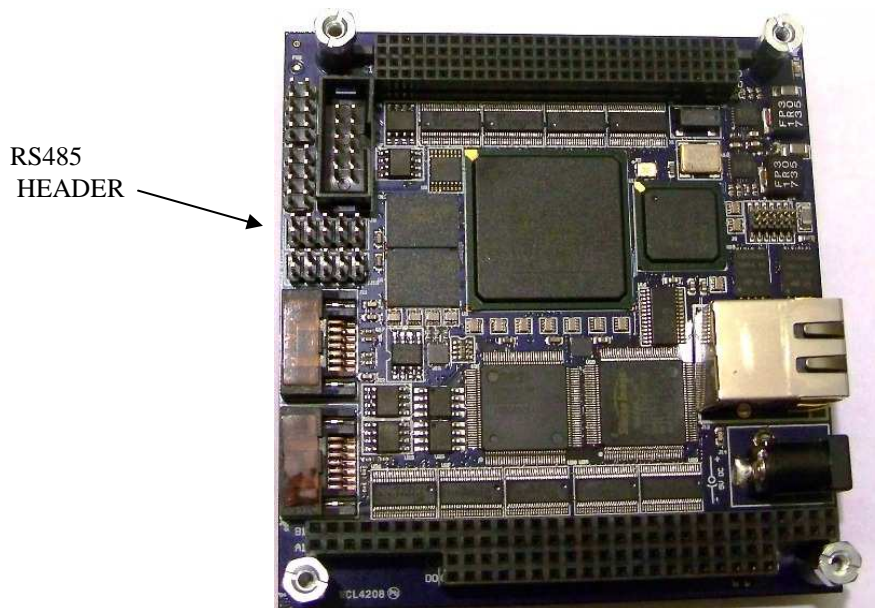


## RS485 Interface

Hollyush2 supports four half duplex, non-isolated, RS485 channels. A termination site is available for each driver/receiver pair and is normally left unpopulated. Each channel is implemented by an SN65HVD11QD Transceiver, each of which has the signals shown below:

| Channel | Signal           | FPGA Pin | Signal | Connector pin |
|---------|------------------|----------|--------|---------------|
| 1       | Data             | G19      | A      | 1             |
|         | Transmit/Receive | J21      | B      | 2             |
| 2       | Data             | D11      | A      | 5             |
|         | Transmit/Receive | P22      | B      | 4             |
| 3       | Data             | J25      | A      | 7             |
|         | Transmit/Receive | J26      | B      | 6             |
| 4       | Data             | A3       | A      | 9             |
|         | Transmit/Receive | H6       | B      | 8             |

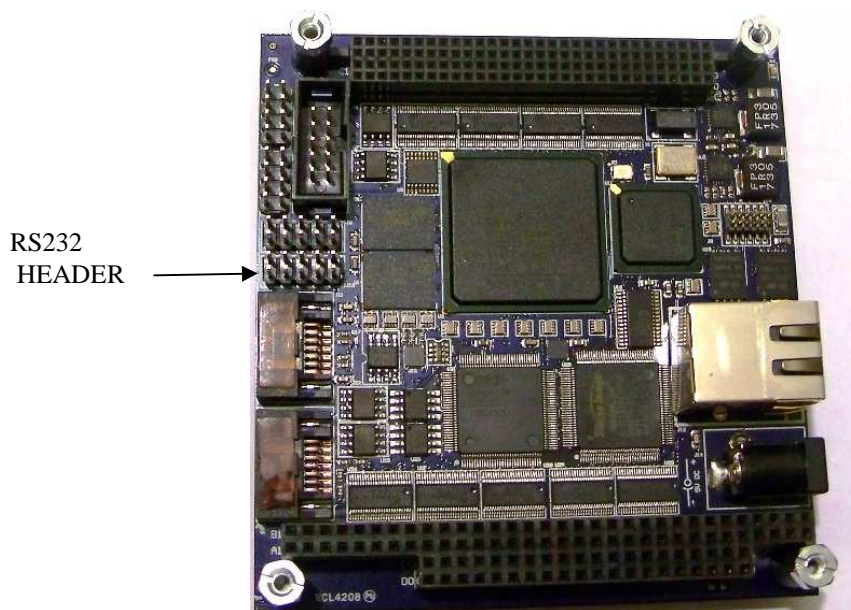
The RS485 connector is a 2 x 5 x 0.1inch header.



## RS232 Interface

Hollybush2 supports an RS232 implementation with hardware handshaking. The board terminates in a 5x2 header and an optional cable and D-Type assembly is available. The device used is a MAX323EIPWR, which has the following pin assignments:

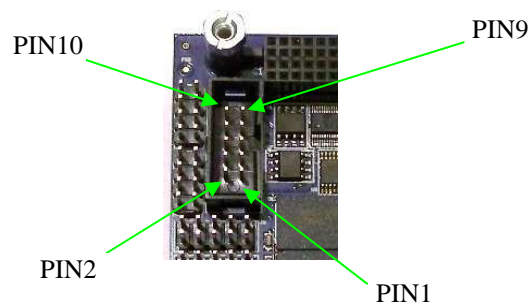
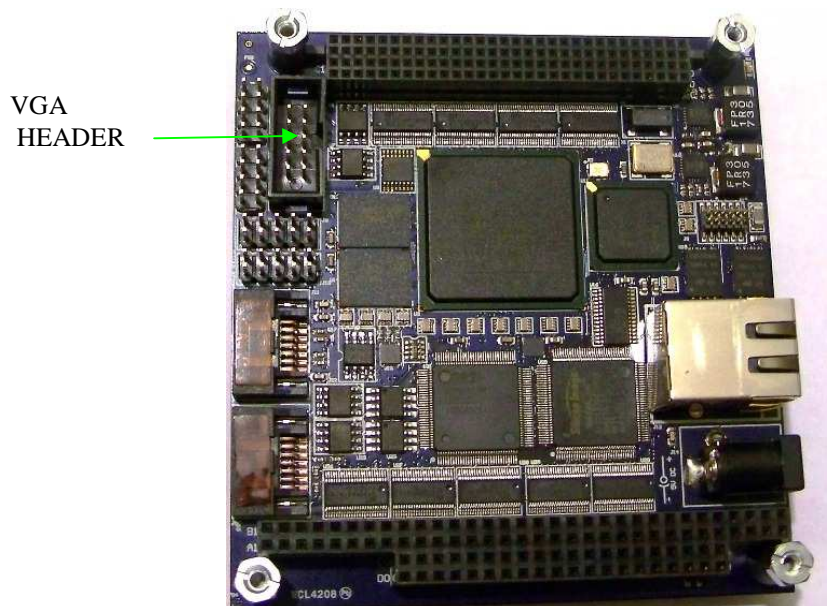
| FPGA Pin | Signal | Max323 pin | Function | Max323 pin | Signal | Connector |
|----------|--------|------------|----------|------------|--------|-----------|
| R21      | DIN1   | 24         | DCD      | 5          | DOUT1  | 1         |
| K18      | DIN2   | 23         | RI       | 6          | DOUT2  | 9         |
| N17      | DIN3   | 22         | RXD      | 7          | DOUT3  | 2         |
| T23      | DIN4   | 19         | CTS      | 10         | DOUT4  | 8         |
| N20      | DIN5   | 17         | DSR      | 12         | DOUT5  | 6         |
| R17      | ROUT1  | 21         | TXD      | 8          | RIN1   | 3         |
| Y26      | ROUT2  | 20         | RTS      | 9          | RIN2   | 7         |
| P18      | ROUT3  | 18         | DTR      | 11         | RIN3   | 4         |



## VGA

A simple VGA implementation is supported on Hollybush2 by a 2 X 5 X 0.1inch shrouded header connector and simple filters. To operate as a VGA port it requires FPGA logic that suitably modulates the VGA control and data signals.

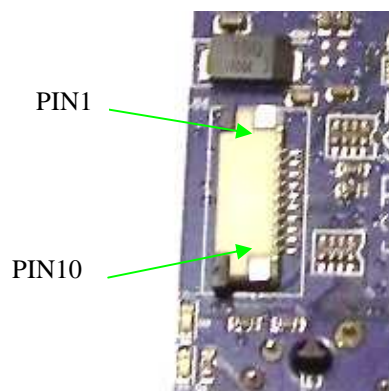
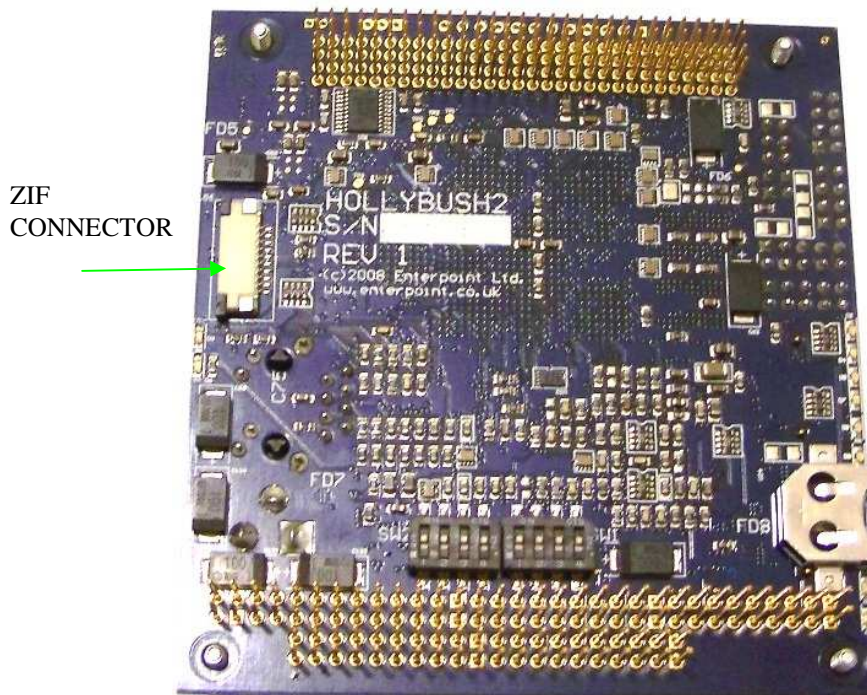
| Signal | FPGA pin | Connector pin |
|--------|----------|---------------|
| RED    | AA10     | 1             |
| NC     |          | 2             |
| GREEN  | AF10     | 3             |
| NC     |          | 4             |
| BLUE   | V12      | 5             |
| DGND   |          | 6             |
| HSynch | AE10     | 7             |
| DGND   |          | 8             |
| VSynch | E12      | 9             |
| DGND   |          | 10            |



## ZIF Connector

On the back of the Hollybush2 there is a 10 pin Zero Insertion Force (ZIF) Connector with 4 General Purpose IOs routed to it from the FPGA. One possible use for this is to connect a keyboard to the Hollybush2. The connections to the FPGA are:

| ZIF Connector | FPGA |
|---------------|------|
| 1             | K23  |
| 2             | DGND |
| 3             | K24  |
| 4             | DGND |
| 5             | H24  |
| 6             | DGND |
| 7             | H26  |
| 8             | DGND |
| 9             | 3.3v |
| 10            | 5V   |



## Power Inputs and Power Supplies

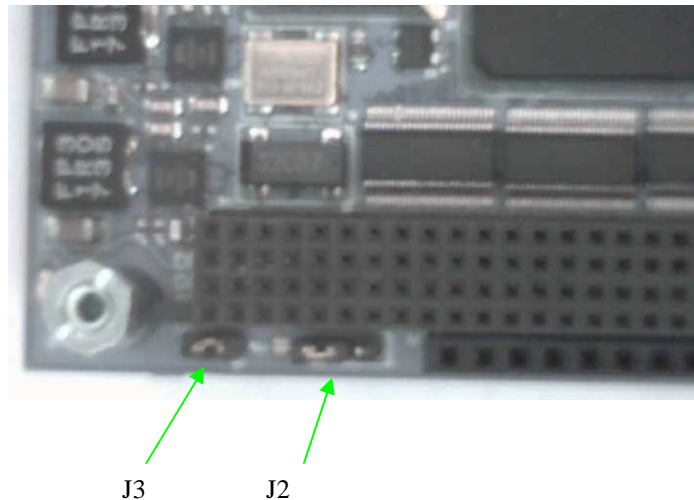
Hollybush2 uses the 5V input from the PC104+, PCI104 or 5v Power Jack socket to generate other on-board voltages. **DO NOT EXCEED 5V. The MIC22600 regulators will not withstand input voltages higher than 5.5v. Please ensure your 5V supply will not overshoot.**

Two MIC22600 regulator devices are used to supply 3.3v for VCCAUX within the Spartan™-3A and 1.2V for the core voltage VCCINT. 3v3 is also used as the IO voltage for banks 0, 1 and 2.

The Power supply to the DDR2 SDRAM (Bank 3) is 1.8V. This is derived from the 5v rail by an Empirion EP538QI regulator. The reference voltage for the DDR2 is 0.9V which is derived from the 1.8V supply by an LP2996 regulator.

**WARNING – THE REGULATORS CAN GET VERY HOT IN NORMAL OPERATION ALONG WITH THE BOARDS THERMAL RELIEF. PLEASE DO NOT TOUCH OR PLACE HIGHLY FLAMABLE MATERIALS NEAR THESE DEVICES WHILST THE HOLLYBUSH2 BOARD IS IN OPERATION.**

There are 2 jumpers fitted on the board just above the 4 x 30 way PCI connector:



J3 links the 3.3V supply from the regulator to the rest of the board. It should normally be fitted.

J2 is used to select the IO voltage supplied to the PCI header (pins A2, B6,C19, D23 and B25). This can be selected as either 3.3v or 5v. The image above shows the jumper fitted in the left position, which selects 3.3v. If 5v is required the jumper should be moved to the right hand side.

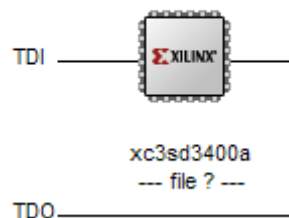
## Programming Hollybush2

The programming of the FPGA and SPI Flash parts on Hollybush2 is achieved using the JTAG interface. Principally it is anticipated that a JTAG connection will be used in conjunction with Xilinx ISE software although other alternatives do exist including self re-programming. The Spartan-6 series needs to be programmed using ISE 9.2 or higher. Versions of ISE prior to 9.2 do not support Spartan-3A. The free Webpack version of the Xilinx tools can be used to program the Hollybush2.

There is a single JTAG chain on Hollybush2. The JTAG chain allows the programming of the Spartan-3A and SPI Flash device.

Using iMPACT Boundary Scan the JTAG chain appears like this:

Right click device to select operations



**Hollybush2 JTAG CHAIN.**

### **1. Programming the FPGA directly.**

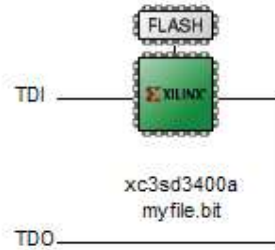
Direct JTAG programming of the Spartan-6 FPGA is volatile and the FPGA will lose its configuration every time the board power is cycled. For sustained use of an FPGA design programming the design into the Flash memory is recommended (see 2 and 3 below).

Direct JTAG programming using .bit files is useful for fast, temporary programming during development of FPGA programs. Right click the icon representing the Spartan-6 FPGA and choose 'Assign New Configuration File'. Navigate to your .bit file and choose 'OPEN'. The next dialogue box will offer to add a flash memory and you should decline. Right click the icon representing the Spartan-3A FPGA and choose 'Program'. On the next dialogue box ensure that the 'Verify' box is not checked. (If it is you should uncheck it, failure to do this will result in error messages being displayed). Click OK. The Spartan-3A will program. This process is very quick (typically one second)

### **2. Programming the SPI flash memory using Boundary Scan.**

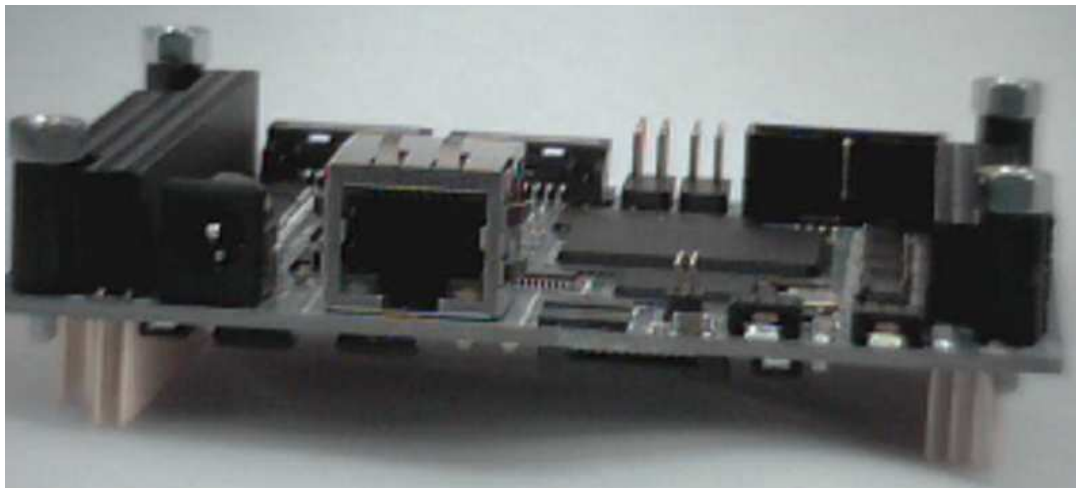
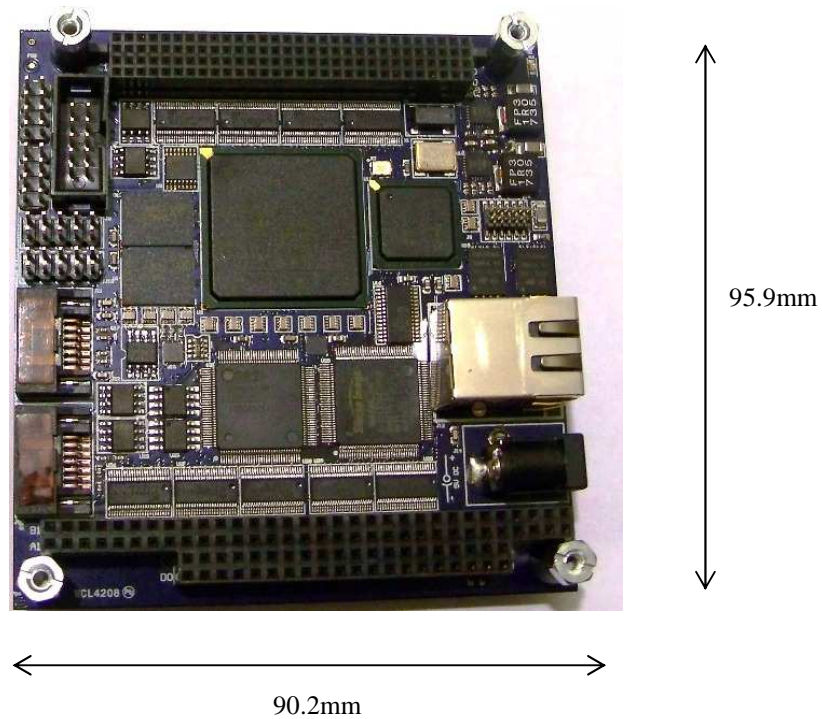
Once the SPI Flash memory has been programmed, the Spartan-3A device will automatically load from the Flash memory at power up. Generation of suitable Flash memory files (.mcs) can be achieved using ISE iMPACT's Prom File Formatter.

Right click on the icon representing the Spartan-3A and choose 'Add SPI/BPI Flash' Navigate to your programming file (.mcs) and click OPEN. Use the next dialogue box to select SPI flash and M25P128. (Data width should be set to 1 on higher versions of iMPACT). The flash memory should appear as shown below.



Right click on the icon representing the flash memory and choose 'program' to load your program into the device. It is recommended that options to 'Verify' and 'Erase before programming' are chosen. Otherwise all defaults can be accepted. The programming operation will take some time (at least 3 or 4 minutes)

## Mechanical Information



HB2 side view

The height of Hollybush2 depends upon the style of connectors fitted. Typically the height measured from the lower surface of the PCB to the top of the Ethernet socket is approximately 12mm. The length of the pins measured from the top surface of the PCB is approximately 12.5mm.

## **Medical and Safety Critical Use**

Hollybush2 boards are not authorised for the use in, or use in the design of, medical or other safety critical systems without the express written person of the Board of Enterpoint. If such use is allowed the said use will be entirely the responsibility of the user. Enterpoint Ltd accepts no liability for any failure or defect of the Hollybush2 board, or its design, when it is used in any medical or safety critical application.

## **Warranty**

Hollybush2 comes with a 90 return to base warranty.

Other specialised warranty programs can be offered to users of multiple Enterpoint products. Please contact sales on [boardsales@enterpoint.co.uk](mailto:boardsales@enterpoint.co.uk) if you are interested in these types of warranty,

## **Support**

Enterpoint offers support during normal United Kingdom working hours 9.00am to 5.00pm. Please examine our Hollybush2 FAQ web page and the contents of this manual before raising a support query. We can be contacted as follows:

|           |  |
|-----------|--|
| Telephone | - +44 (0) 121 288 3945   |
| Email     | - <a href="mailto:support@enterpoint.co.uk">support@enterpoint.co.uk</a> |