



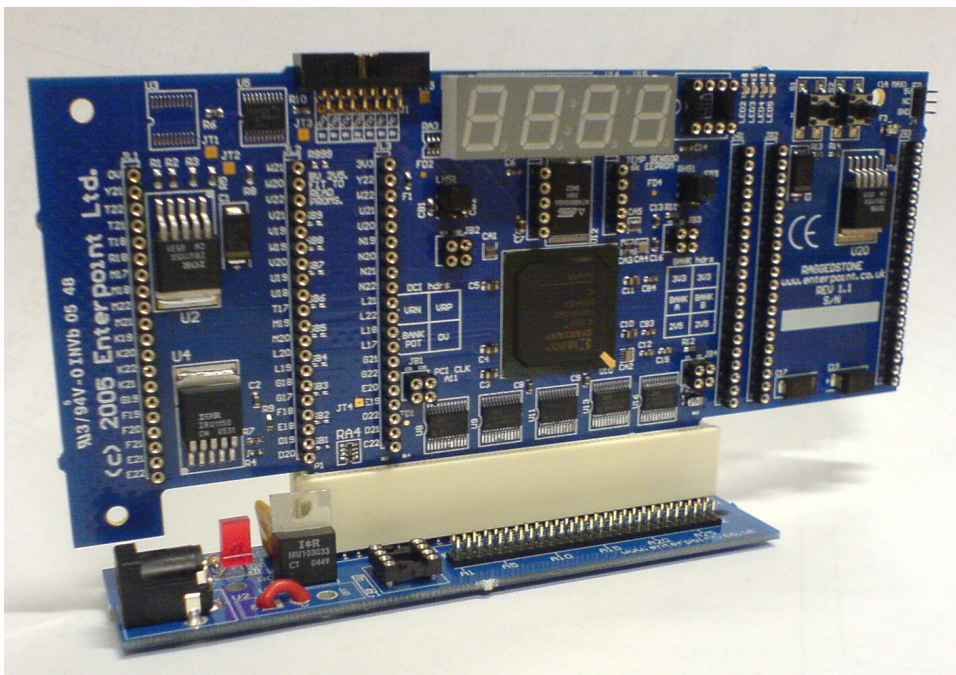
## **PCI I/O expansion and power module, (Rev2.1)**

This document will give a brief description of our new PCI expansion module (PCIEM), our new PCIEM has been designed to work for all of Enterpoint's Spartan-3 development boards.

### **FEATURES:**

- 2.1mm DC jack, to receive a common 5V 5A power brick,
- 5A resettable polyfuse to limit the current provided to the development board,
- A IRU1030-3.3 fix output regulator,
- Status LED indicator,
- Oscillator socket of 8-pin dill oscillators,
- 27\*2 2mm header for the I/O expansion from the development board,
- PCI connection header.

With the correct DC power brick attached one can provide the two main voltages required in the standard PCI specification the input is tracked such that it first reaches the polyfuse. The polyfuse, which limits the total current to 5A, this then goes of to provide 5V's to the development board and the IRU regulator, which generates the 3V3. Also hanging of the polyfuse output is a status LED, which turns on when power is provided to the PCI edge connector, and a 5V oscillator socket with a localised but not populated capacitor for decoupling. As a measure of protection a diode is also wired in to provide protection of surges on the board, as to protect the development board.



**CAUTION:**

Only 5V DC power brick are advised due to the direct feed to the development board, LED and oscillator. Anything other than what is recommended will result in to great a voltage seen by the FPGA development board and hence permanent damage will ensue.

Warning the oscillator is tracked to the 2mm header in position B1 which is then tracked through to the PCI edge connector in the same position as the PCI clock found in the PCI specification.

**PCI I/O expansion header pin out.**

Header PIN	PCI signal		Raggedstone1	Broarddown2	Min-can
A1	INTA		B19	M3	M3
A2	RST_I		A19	F2	F2
A3	GNT_I		D18	L3	L3
A4	PME_N		n/a	n/a	n/a
A5	AD_IO_30		A18	H5	H5
A6	AD_IO_28		B17	G3	G3
A7	AD_IO_26		D17	G1	G1
A8	AD_IO_24		D15	H1	H1
A9	IDSEL_I		D14	L5	L5
A10	AD_IO_22		F12	J4	J4
A11	AD_IO_20		B15	J5	J5
A12	AD_IO_18		A14	J1	J1
A13	AD_IO_16		F17	K5	K5
A14	FRAME_IO		C13	M2	M2
A15	TRDY_IO		B13	M1	M1
A16	STOP_IO		A12	L2	L2
A17	PAR_IO		A9	N4	N4
A18	AD_IO_15		B10	K4	K4
A19	AD_IO_13		A8	K2	K2
A20	AD_IO_11		F11	N5	N5
A21	AD_IO_9		F10	P1	P1
A22	CBE_IO_0		F9	N2	N2
A23	AD_IO_6		D7	P5	P5
A24	AD_IO_4		C6	R2	R2
A25	AD_IO_2		E6	R5	R5
A26	AD_IO_0		A5	T2	T2
A27	No connection		n/a	n/a	n/a
B1	CLK_PCI		A11	B11	B11
B2	REQ_Q		C18	L6	L6
B3	AD_IO_31		B18	G5	G5
B4	AD_IO_29		E17	G4	G4
B5	AD_IO_27		C17	G2	G2
B6	AD_IO_25		E15	H2	H2
B7	CBE_10_3		E13	M5	M5

B8	AD_IO_23		F13	H4	H4
B9	AD_IO_21		A15	J6	J6
B10	AD_IO_19		B14	J2	J2
B11	AD_IO_17		F16	K6	K6
B12	CBE_10_2		D13	M6	M6
B13	IRDY_IO		A13	L1	L1
B14	DEVSEL_IO		E12	L4	L4
B15	LOCK		n/a	n/a	n/a
B16	PERR_IO		D12	N3	N3
B17	SERR_IO		B12	M4	M4
B18	CBE_10_1		C10	N1	N1
B19	AD_IO_14		B9	K3	K3
B20	AD_IO_12		E10	K1	K1
B21	AD_IO_10		E9	N6	N6
B22	AD_IO_8		B8	P2	P2
B23	AD_IO_7		E7	P4	P4
B24	AD_IO_5		B6	R1	R1
B25	AD_IO_3		D6	P6	P6
B26	AD_IO_1		B5	T1	T1
B27	M66EN		n/a	n/a	n/a

## PCI I/O schematic.

