

PCI™ to OPB™ Bridge Core



Principal Features

32Bit, 33MHz PCI™ to 32Bit 33Mhz OPB™
PCI 2.2 Compatible.
Small size –800-1200 Slices in Xilinx™
Spartan™-3.
Target and Initiator Capability.
Tight coupled OPB bus – direct interface.
1-6 BARs supported.
Memory or I/O on all BARs
Burst data transfer – Target or Initiator
Target mode address translation on all BARs.
Initiator mode address translation.
PCI™ and OPB™ retry mechanisms support.
Target and Initiator Aborts supported.
Custom Vendor ID, Device ID, Class ID can be supported.
Multiple pseudo device support available.
Netlist or VHDL source licensing available.
VHDL testbench available
Non-US origin – not subject to US EAR.

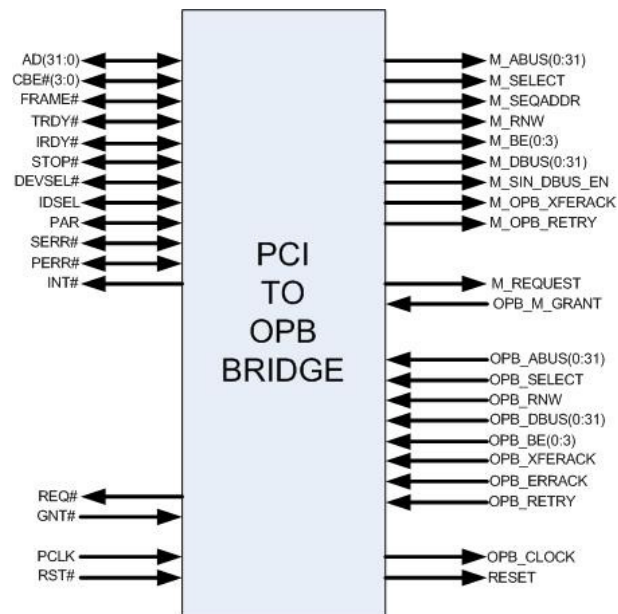


Figure 1-Simplified Bridge Pinout

The PCI™ to OPB™ Bridge Core offers a versatile and easy connection solution to connect PCI™ to a simple OPB™ bus interface. Using OPB™ based peripheral IPs new system designs can be implemented in minutes using a simple OR array for connectivity.

The core offers a competitive solution in features and size compared to competing products and has been optimized for the Xilinx™ Spartan™-3 FPGA families for low cost applications. Other Xilinx™ FPGA families are supported include Virtex™-II, Virtex™-IIPro, Virtex™-4, Virtex™-5. Other FPGA and ASIC technologies can be supported. Please contact sales for these other technologies.

Customer application specific optimizations can be offered for minimum size for a small charge. We can also offer alternate backend interfaces for additional cost.

The core is available in a range of licensing options including Target only netlist, Target and Initiator Netlist and Full Source Code options. Low cost small volume licenses also available.

Full design and consultancy service available for FPGA, PCB and software design based on this core. Extended support contracts are also available. On-site training in the use of core and PCI can also be offered.