



Drigmorn1 User Manual

Issue – 1.00

Kit Contents

You should receive the following items with you Drigmorn1 development kit:

- 1 - Drigmorn1 Board,
- 2 – Prog2 Programming Cable (not with OEM).
- 3 – Power Supply (Option).

Foreword

**PLEASE READ THIS ENTIRE MANUAL BEFORE PLUGGING IN
OR POWERING UP YOUR DRIGMORN1 BOARD.
PLEASE TAKE SPECIAL NOTE OF THE WARNINGS WITHIN
THIS MANUAL.**

Trademarks

Coolrunner-II, Spartan, ISE, EDK, Webpack, Xilinx are the registered trademarks of Xilinx Inc, San Jose, California, US.

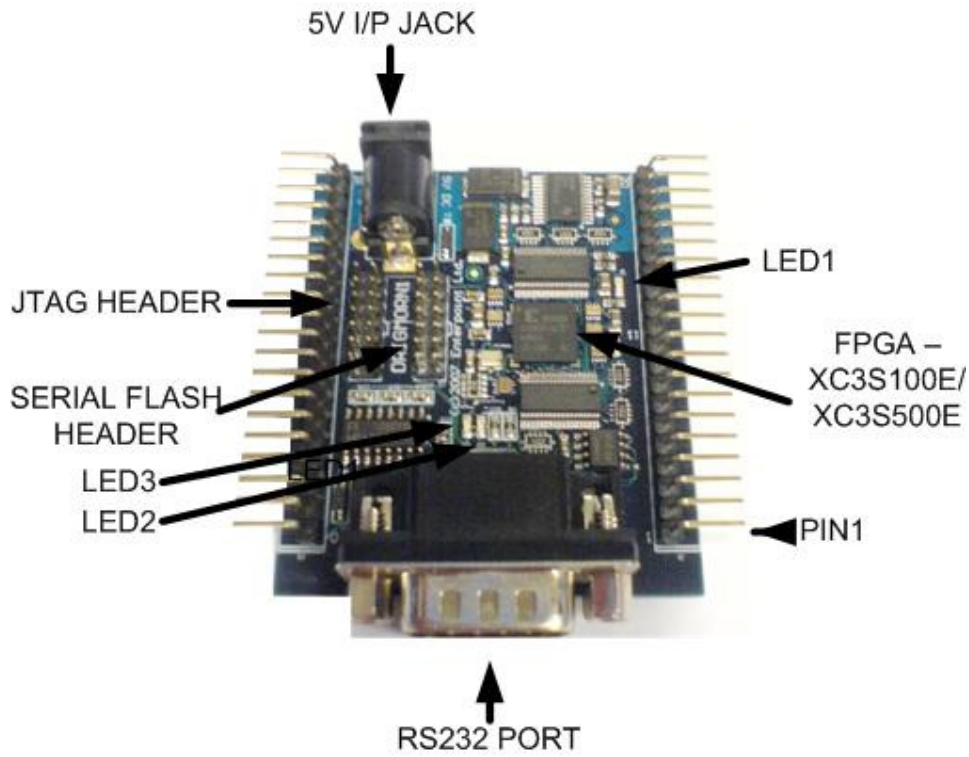
Drigmorn1 is a trademark of Enterpoint Ltd.

Introduction

Welcome to your Drigmorn1 board. Drigmorn1 is a low cost high performance Spartan™-3E FPGA based development board.

The aim of this manual is to assist in using the main features of Drigmorn1. Should this manual fail to explain a feature sufficiently then our support team can be reached by email on support@enterpoint.co.uk.

Finding Your Way Around



Getting Started

Your Drigmorn1 normally comes with our Waggle Test build loaded. The source VHDL and constraints file (UCF) are available on our website on the Drigmorn1 Applications Page:

http://www.enterpoint.co.uk/component_replacements/drigmorn1_apps.html

This application will cause all of the LEDs to flash and all of the I/O on the Gull Wing Connectors to be configured as outputs and to toggle (at different rates per pin).

The RS232 port implements a loopback from RXD to TXD. Using a terminal emulator on a PC with a COM Port setting at between 2,400 and 115,200 baud you should see typed characters echoed back on the screen (double if local echo is on)

If you are going to plug your Drigmorn1 into another circuit please ensure the Waggle Test is erased from Serial Flash in case of logic drive conflicts.

Some useful links and other information can be obtained from our website here:

<http://www.enterpoint.co.uk/techtips/techtips.html>

Drigmorn1 Features

Power Inputs and Power Supplies

Drigmorn1 uses a notional 5V input but can operate from 3.5V to 5.5V (specification guaranteed) but in practise can operate as low as 2.8V and as high as 6V if care in interfacing signal levels is taken.

The power can be input from the 2.1mm Jack (centre = +5V) or from pin header (pin40 = +5V, pin 20 = 0V/DGND). Input current requirements will depend on the design loaded into the FPGA on the board and I/O loading but normally would be in the range 100-500mA.

An onboard a Texas Instruments TPS70402 linear regulator produces 1.22V and 2.5V from the input supply voltage. The 1.22V is used for the SpartanTM-3E core voltage and the 2.5V is used for all other devices (except RS232 driver) and for the Vccaux/Bank Voltages of SpartanTM-3E.

WARNING – THE REGULATORS CAN POTENTIALLY GET VERY HOT IN SOME UNUSUAL CIRCUMSTANCES ALONG WITH THE BOARDS THERMAL RELIEF. PLEASE DO NOT TOUCH OR PLACE HIGHLY FLAMABLE MATERIALS NEAR THIS DEVICE WHILST THE DRIGMORN1 BOARD IS IN OPERATION.

Selecting the FPGA Bank (VCCIOX) voltages.

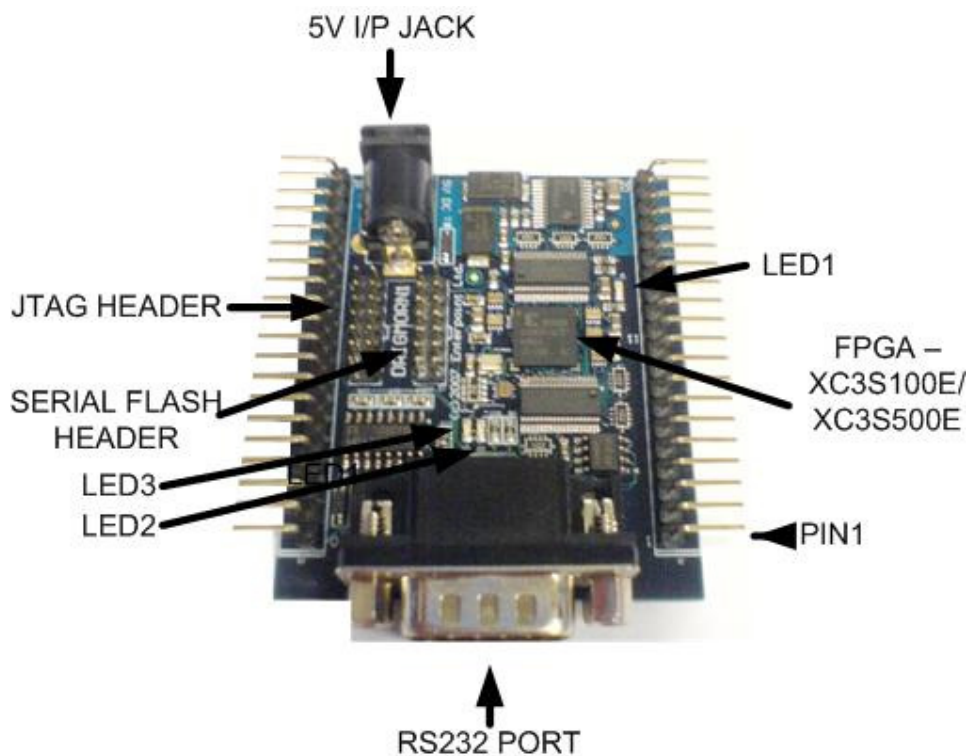
Drigmorn1 fixes the I/O voltages all of FPGA banks to 2.5V. However there are pull-ups to all the I/O pins on the Gull-Wing Connectors to the input supply voltage allow the I/O to achieve CMOS type levels were these are needed.

Programming Drigmorn1

For programming and building your design you will need to download a copy of ISE Webpack™ form Xilinx™. You can obtain it here:

http://www.xilinx.com/ise/logic_design_prod/webpack.htm

The programming of the FPGA and Serial Flash parts on Drigmorn1 are achieved using 2 separate interfaces which appear on the two 2x7 2mm headers on Drigmorn1. The picture below shows their locations. Please take special note of the polarity marks on the board which will correspond to key on your programming cable connector. The cable should be inserted so that the key on the cable is on the same side as the marking on the board. Please also take care that you do not misalign the cable socket to the header by one or more positions.



The first interface is a standard JTAG port which follows the standard layout for our Prog2 cable and for Xilinx Programming Cables IV and later. The Xilinx ISE Impact tool can be used to control programming (boundary scan mode). ISE Webpack can be download free from Xilinx on their website. Direct JTAG programming is volatile and the FPGA will lose its configuration every time the board power is turned off/on. From sustained use of FPGA design programming the design into the Serial Flash memory is recommended. Generation of suitable Serial Flash content files and control of the JTAG chain can be achieved using the ISE Impact.

The second interface contains the signals that connect to Serial Flash and additionally Prog_B. When a Prog2 or suitable Xilinx cable is plugged in Prog_B is connected to DGND/0V and the Spartan™-3E FPGA is placed into the pre-configured state. This avoids conflicts on the Serial Flash control and data lines with drive from the programming cable. The pinout of the header also allows ISE Impact tool (serial flash mode) to program the Serial Flash. Please note to allow the

FPGA to configure you must remove the programming cable from the Serial Flash Programming Header.

FPGA

Drigmorn1 supports Spartan™-3E devices in the CP/CPG132 package. Standard builds of Drigmorn1 use commercial grade devices but industrial grade parts can be fitted at extra cost subject to minimum order quantities and charges. Currently we are supplying only the XC3S100E-4CPG132C and XC3S500E-4CPG132C FPGAs as standard options. The XC3S250E-4CPG132C is also possible.

LEDS

Supplied on Drigmorn1 there are 3 LEDS driven by the FPGA. LED1 has a positive polarity i.e. '1' = on. LED2 and LED3 are negative polarity i.e. '0' = on.

The LEDS are situated on FPGA IO pins as indicated below:

LED	LED1	LED2	LED3
FPGA PIN	C14	P6	P7

CLOCK

Drigmorn1 comes fitted with a 40 MHz oscillator. This is input on FPGA pin M6.

FLASH MEMORY

Supplied as standard on Drigmorn1 is a 4Mbit ST Microelectronics M25P40. This device is used to configure the Spartan™-3E. The remainder of flash memory is available for storing code for PicoBlaze™, MicroBlaze™ or other microprocessors.

A XC3S100E will use 581,344 bits of this memory for configuration. The XC3S500E will use 2,270,208 bits for configuration.

RS232 Port

Drigmorn1 has 2 drivers and 2 receivers for RS232 and connections to these are via the 9 way D-Type connector. A MAX202 driver/receiver is fitted with a capability of up to 200 Kbits transmission speed.

General I/O

Drigmorn1 supports thirty two, 5V tolerant, I/O on its Gull-Wing connectors. The top 2 pins and bottom 2 pins of the Gull-Wings are power pins and the middle 16 of each side are I/O. Pin numbering is over the 2 connectors and counts in an anti-clockwise direction. There are some pin number markings on the board and FPGA pinout constraints file is available on the Applications webpage for Drigmorn1.

Medical and Safety Critical Use

Drigmorn1 boards are not authorised for the use in, or use in the design of, medical or other safety critical systems without the express written person of the Board of Enterpoint. If such use is allowed the said use will be entirely the responsibility of the user. Enterpoint Ltd will accept no liability for any failure or defect of the Drigmorn1 board, or its design, when it is used in any medical or safety critical application.

Warranty

Drigmorn1 comes with a 90 return to base warranty.

Other specialised warranty programs can be offered to users of multiple Enterpoint products. Please contact sales on boardsales@enterpoint.co.uk if you are interested in these types of warranty,

Support

Enterpoint offers support during normal United Kingdom working hours 9.00am to 5.00pm. Please examine our Drigmorn1 FAQ web page and the contents of this manual before raising a support query. We can be contacted as follows:

Telephone	- +44 (0) 1684 585262
Email	- support@enterpoint.co.uk