

Moel-Bryn FPGA, ASIC, SOC, IP Prototyping Systems



Broaddown1 Motherboard

Features

- Supports prototyping or evaluation capability of up to 128M gates using Xilinx Virtex II devices as target.
- Support multiple I/O standards including Analogue, Optical, PECL, LVDS, TTL, CMOS (see note 2).
- External world I/O options allow over 1000 connections.
- Uses ATX PC as host for power supply and optionally control (see note 1). The motherboard may also be operated independently on bench allowing easier probe/logic analyser access.
- 8 daughterboard positions available, in a 4x2 array, for prototyping array.
- Flexible mixing of daughterboards.
- 4 fixed clock oscillators for direct use (via Routing FPGA).
- 8 user (8 pin dip) useable clock oscillators for direct use (via Routing FPGA).
- 8 analogue PLL clock multipliers for clock multiplication with low jitter.
- Further DLL clock multiplication/division available in Spartan2 (PCI FPGA) /Spartan2E (Routing FPGA) devices.
- Daughtercard support for multiple I/O standards.
- On board generation of power supplies +3.3V, +2.5V, +1.8V, +1.5V, -5V.
- Two additional variable positive power supplies for termination voltages.
- Capacitor backup supply to support encryption keys in Swinyard daughterboards (allows evaluation of IP fixed to target daughterboard key programmed by IP vendor).
- JTAG programming of daughterboards for development.
- JTAG reprogrammable prom for motherboard FPGAs (separate JTAG chain to daughterboards for security).
- Socketed single parallel flash memory for programming daughterboard FPGAs.

- Initial daughterboards available with XC2V1000 (Swinyard 10004/5), XC2V3000 (Swinyard 30004/5), XC2V6000 (Swinyard 60004/5) parts.
- Routing supplied for 1 clock connection between each adjacent daughterboard (each direction).
- Up to 20000 Mbyte/s directly connected bandwidth between adjacent daughterboards .
- LVDS serialiser/ deserialiser available for signal fanin/ fanout on inter-daughterboard links.
- Addition bypass connections available between any daughterboards. Routing FPGA allows programming and use of these bypass connections.
- Hardware support for Temperature measurement using Virtex II thermal diode for each daughterboard.
- Hardware support for software reporting of daughterboard types.
- Optional design assistance, debug and consultancy available.
- Pass through daughterboards available for maximizing I/O use.

Note(1) – The motherboard exceeds the standard PCI card physical specifications. We have checked various ATX tower cases (midi and full tower) and found only minor cable routing problems in the cases that we inspected. Careful selection of PCI slot will minimize these problems. Please check the space available in your host system before purchase. It is also advisable to check the rating of the power supply. If it is less than 300W, or 400W if Athlon or Pentium 4 based, then swap the supply for one of greater capacity. Please contact Enterpoint for advice on cases or power supplies if unsure.

Note(2) - There can be some incompatibilities with other LVPECL devices when used in conjunction with Virtex II devices. Please see Virtex II datasheet for details.

Planned Additional Features

- Daughterboard programming via PCI bus.
- Temperature measurement and control via software I/F.
- Analogue front/back end daughterboards.
- Ultra deep FIFO daughterboards.
- Strongarm daughterboard.
- DDR memory daughterboard.
- Addition Virtex II daughterboards (sizes and speed grades).
- Piggyback daughterboard adding up to 8 additional Virtex II devices.

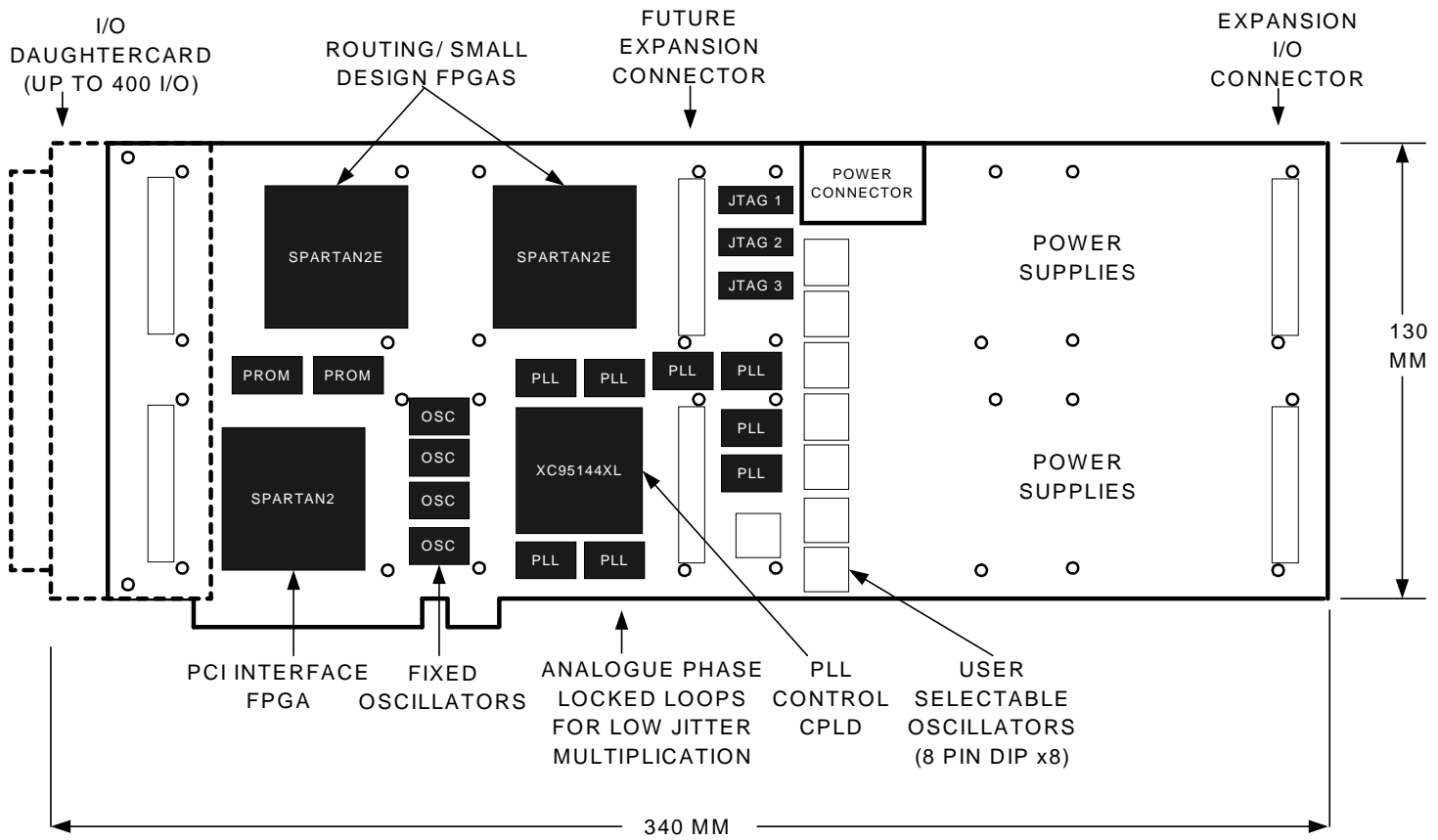
General Description

The Moel-Bryn prototyping system offers the SOC or IP designer the ultimate off the shelf design target. The standard fitment of up to 8 daughterboards will allow up to 64 million user gates of design to be implemented on the Broaddown1 motherboard. Using suitable daughterboards can also allow the prototyping system to deal with real world analogue signals a feature omitted in many competing systems.

Other features which make the Broaddown1 superior is the use of the latest Virtex II FPGAs for the daughterboards. Each of these devices can support up to 8 global/secondary clocks allowing up to 64 clocks in one design using all daughtercards. Should the design exceed these clock limits then addition clocks can be implemented using local routing (for very experience designers only). Additionally up to 144 multiplier and 144 block rams are available using XC2V6000 in each daughterboard.

Using the Virtex II daughterboards with pass daughtercards will allow the maximizing of I/O functions. Arrays of 4x1 or 2x2 or 3x2 or even unusual patterns of Swinyard modules can be used with no penalty. This feature allows the breakdown of logic to approximate that in the final product asic and allowing access to internal signals.

BROADDOWN1 – Back Side (Unpopulated)



BROADDOWN1 – Front Side

